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OSFP MSA

Specification for

OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

Rev 5.1

September 12th, 2024

Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, and mechanical and thermal requirements of the OSFP Module, connector, and cage systems. The OSFP Management interface is described in a separate document: “Common Management Interface Specification (CMIS)”.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Revision History:

Rev5.1	9/12/2024	Section 3, Reference design of a larger label on the module front is added (Figure 3-5). Section 6, OSFP1600 footprint is updated to provide the plated pads under the connector plastic standoff. Section 7.3, 19.9mm pitch OSFP stacked SMT connector is added. Section 7, cage latching flap minimum length is added. Section 13, PMD and optical connector lane assignments are updated, including addition of SN-MT and MMC connector examples. Appendix E, F and G are added.
Rev 5.0	10/2/2022	Section 4 is added for the OSFP1600. In Section 5.8 and 5.10, tolerances are updated for OSFP1600. Section 8 is added for the cabled host footprint. Section 12.3 added for OSFP1600 PMDs. Section 13 (Electrical Interface) is updated to support OSFP1600.
Rev 4.1	8/2/2021	Cage latch flap radius is enlarged. Cage shoulder keepout added to the stacked SMT cage (Sec 5). Cage assembly tolerance is relaxed (Sec 5).
Rev 4.0	5/28/2021	Type 2 and 3 modules with bigger front are added (Fig 3-3). Module latch release feature is further clarified (Sec 3.7). Optional riding heatsink is added (Sec. 4.5). Case temperature location requirement and connector environmental requirement are added (Sec. 8). OSFP-RHS nose shape is updated to avoid a potential interference with a connector (Fig 9-8). OSFP-RHS heatsink contact area is adjusted (Sec. 9). OSFP800 specification is added, with PMDs (Sec. 10.2) and electrical information (Sec. 11.4). More optical connector configurations are added (Section 10.3). Max current to the module is increased to 10A, supporting 30W module (Sec. 11.6). Lower power mode is added to allow up to 2W (Table 11-8).
Rev 3.0	3/14/2020	Specifications for the stacked SMT connector and its cage are added to section 5. Reference design of cage vent holes are added to SMT single row cage. Universal MIS is added to the reference section.
Rev 2.0	1/14/2019	Major updates including: Touch temperature (section 3.9), stacked cage/connector (section 5), OSFP-RHS (section 8) and informative pull tab length (Appendix B) are added. Impedance requirement for the OSFP is relaxed (section 7.2). Management interface speed is increased (Section 10.5). Power class definition are updated, with increase of max power to 21.1W (section 10.6). GD&T of the drawings are updated. MPO-12 two row and MPO-16 lane assignments are added (section 9.8).
Rev 1.12	8/1/2017	Editorial updates, as of: Note 1 in the Figure 1 is clarified with “0.00mm max from top”. PMD in the section 7 and titles are updated, including Figure 49 and 50 the optical receiver/transmitter lane numbers are revised to avoid any confusion. In section 8, word “must” be replaced with “shall”. Legal claim at page 1 “fitness or any..” typo fixed as “fitness for any..”.
Rev 1.11	6/26/2017	Editorial updates, as of: Typo in the figure number in the figure table of contents fixed; Revision history added.

Rev 1.1	6/7/2017	Minor updates, as of: MPO 24 lane assignment (section 7.7.3) removed, to remove conflict with other industry conventions ; PCB location with respect to the module is specified with MMC modifier, to provide better dimensional control (Figure 8) ; Test ambient condition (20C, sea level) specified for the clarification in the module airflow impedance (Figure 42) ; In section 8.5, “optional” added to the fast and high-speed bus mode to clarify that those modes are optional ; In table 8-6, T_hplp description is updated for better clarification of the feature ; Power filter inductance adjusted to increase the power supply margin (Figure 59)
Rev 1.0	3/17/2017	Initial Release

Table of Contents

Table of Figures

Tables

1 Scope

The OSFP specification defines:

- The OSFP module mechanical form factor, including the latching mechanism;
- The host cage together with the mating connector;
- The electrical interface, including pin-out, data, control, and power and ground signals;
- The mechanical interface, including the package outline, front panel, and printed circuit board (PCB) layout requirements;
- Thermal requirements and limitations, including heat sink design and airflow;
- Electrostatic discharge (ESD) requirements;
- The module management interface as contained in the Common Management Interface Specification (CMIS).

2 References

- IEC 61754-7-1:2014: Fibre optic interconnecting devices and passive components – Fibre optic connector interfaces – Part 701: Type MPO connector family – One fibre row
- IEC 61754-20:2012: Fibre optic interconnecting devices and passive components – Fibre optic connector interfaces – Part 20: Type LC connector family.
- TIA-604-18, FOCIS 18 Fiber Optic Connector Intermateability Standard – Type MPO-16
- TIA-604-19, 2021 Edition, July 30, 2021 – FOCIS 19 Fiber Optic Connector Intermateability Standard- Type Sen Connector
- SFF-8636: Specification for Management Interface for Cabled Environments, Rev. 2.11, January 03,2023
- UM10204, I^{2}C-bus specification and user manual, Rev 7 – 1 OCT 2021
- MIPI I3C^{SM} HCI^{SM} v1.2, MIPI Alliance, April 2023
- SFF-8679: Specification for QSFP+ 4X Base Electrical Specification, Rev 1.8 October 4, 2018
- SFF-8024: Specification for SFF Module Management Reference Code Tables, Rev 4.12, July 9, 2024
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
- ANSI/ESDA/JEDEC JS-001-2023: ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level
- IEEE802.3bs: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation
- IEEE802.3cd: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation
- IEEE802.3bj: Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables
- IEEE802.3bm: Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables
- IEEE802.3ck: Amendment 4: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling

- EIA-364-70: Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
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- UL 62368-1, Standard for Audio/video, information and communication technology equipment – Part 1: Safety requirements, Edition 3, 2019
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- Interface Specification for MDC Receptacle, Rev 4, February 6 2020, USC11383001, US Conec
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- Specification for SN® Transceiver Receptacle, SN® Connector Specification SN60092019 Rev 1.1, Senko
- OIF-CMIS-05.2, Common Management Interface Specification (CMIS), Revision 5.2, Optical Internetworking Forum, https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.2.pdf
- OIF-CEI-05.2, Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps, and 112G+ bps I/O, 2024, Optical Internetworking Forum, https://www.oiforum.com/wp-content/uploads/OIF-CEI-05.2.pdf
- Press Release, AirMT™ series Non-contact MT Technology, https://global-sei.com/company/press/2019/09/prs072.html
- 3M™ Expanded Beam Optical Connector (EBO), https://www.3m.com/3M/en_US/data-center-us/applications/interconnect-optical/
- USConec MXC® Expanded Beam Connector, https://www.usconec.com/connectors/mxc-expanded-beam
- USConec MMC connector, https://www.usconec.com/featured-products/mmc-connector
- Specification for OSFP-XD, Octal Small Form Factor eXtra Dense Pluggable Module, Rev 1.1, OSFP MSA, https://osfpmsa.org

3 OSFP Module Mechanical Specification

For OSFP1600 (the OSFP module that supports 200G per lane), see section 4. For OSFP or OSFP800, which support 50G or 100G per lane, either of the mechanical specifications in this section or section 4 are applicable.

3.1 Overview

A typical OSFP module is shown in Figure 3-1. An assortment of connector types is shown. Connector and cable variations not shown here are allowed, including as depicted in section 13.4.

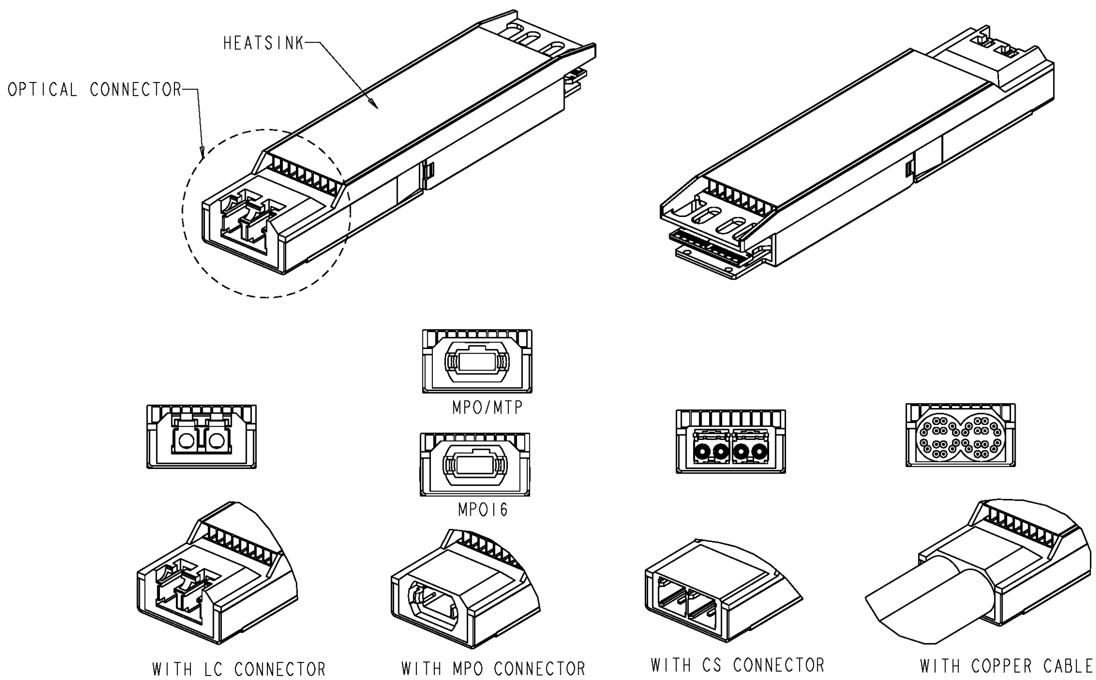


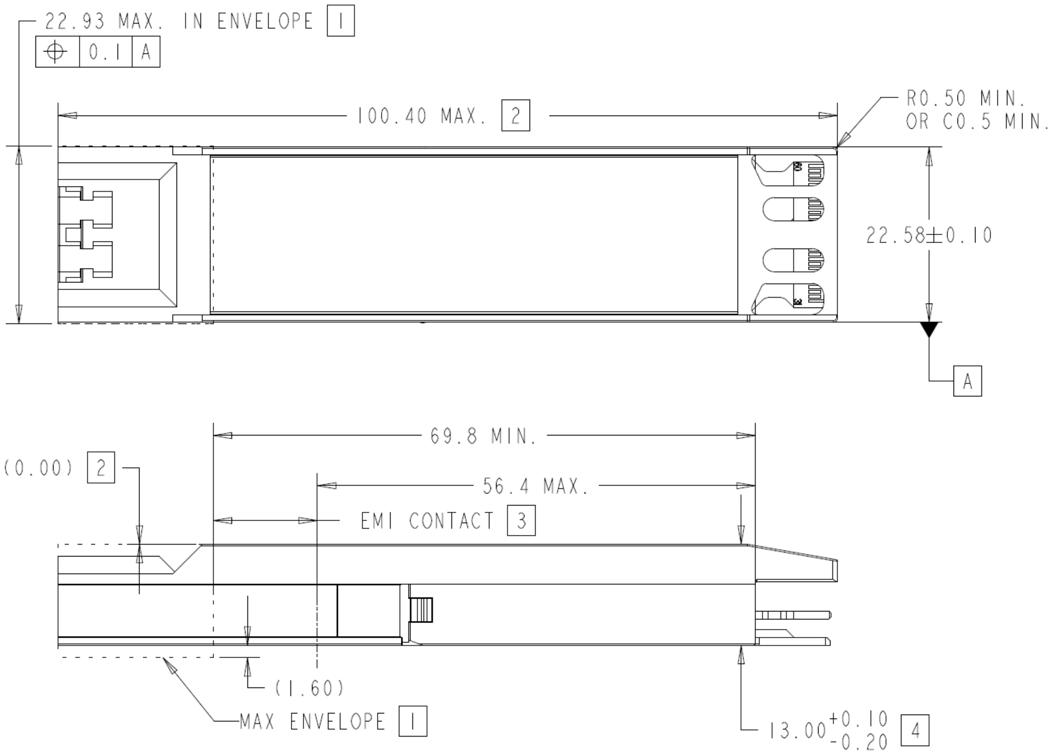
Figure 3-1: OSFP module with different connectors (Duplex LC, MPO, CS®, Copper)

In the module's mechanical drawings included throughout this specification, the datum defined in Table 3-1 will apply.

Table 3-1: Descriptions of the module mechanical datum

Designator	Description	Figure
A	Width of the Module	Figure 3-2
B	Forward stop of the Module	Figure 3-2; also see Figure 3-10
C	Bottom surface of the Module	Figure 3-2
D	Width of the Module's PCB	Figure 3-21
E	Signal pad leading edge of the Module's PCB	Figure 3-21
F	Top surface of the Module's PCB	Figure 3-21

Figure 3-2 shows the dimensions of the Standard OSFP module. Note that the module is shown with a typical latch release mechanism without a pull tab. Alternate latch release mechanisms are allowed. All dimensions in this specification are in millimeters (mm) unless otherwise noted.



NOTES:

1 FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.6MM MAX FROM THE BOTTOM OF THE MODULE AND CAN HAVE UP TO 22.93mm WIDTH IN THE MAX ENVELOPE SHOWN.

2 APPLIES TO TYPE 1 AND TYPE 2 MODULES; NOT APPLIES TO TYPE 3 MODULE.

3 INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

4 APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

Figure 3-2: OSFP overall dimensions

Figure 3-3 shows the total length and front height of Type 1, Type 2, and Type 3 OSFP modules. A Type 2 OSFP module provides maximum of 16mm of additional length in the front compared to a Type 1 module. A Type 3 OSFP module provides maximum of 3.6mm of additional height in the front compared to a Type 2 module. Type 2 and Type 3 modules can provide additional space for various optical interfaces, as described in the section 13.4. Type 3 OSFP modules are incompatible with the stacked cages in discussed in sections 7 and 8.

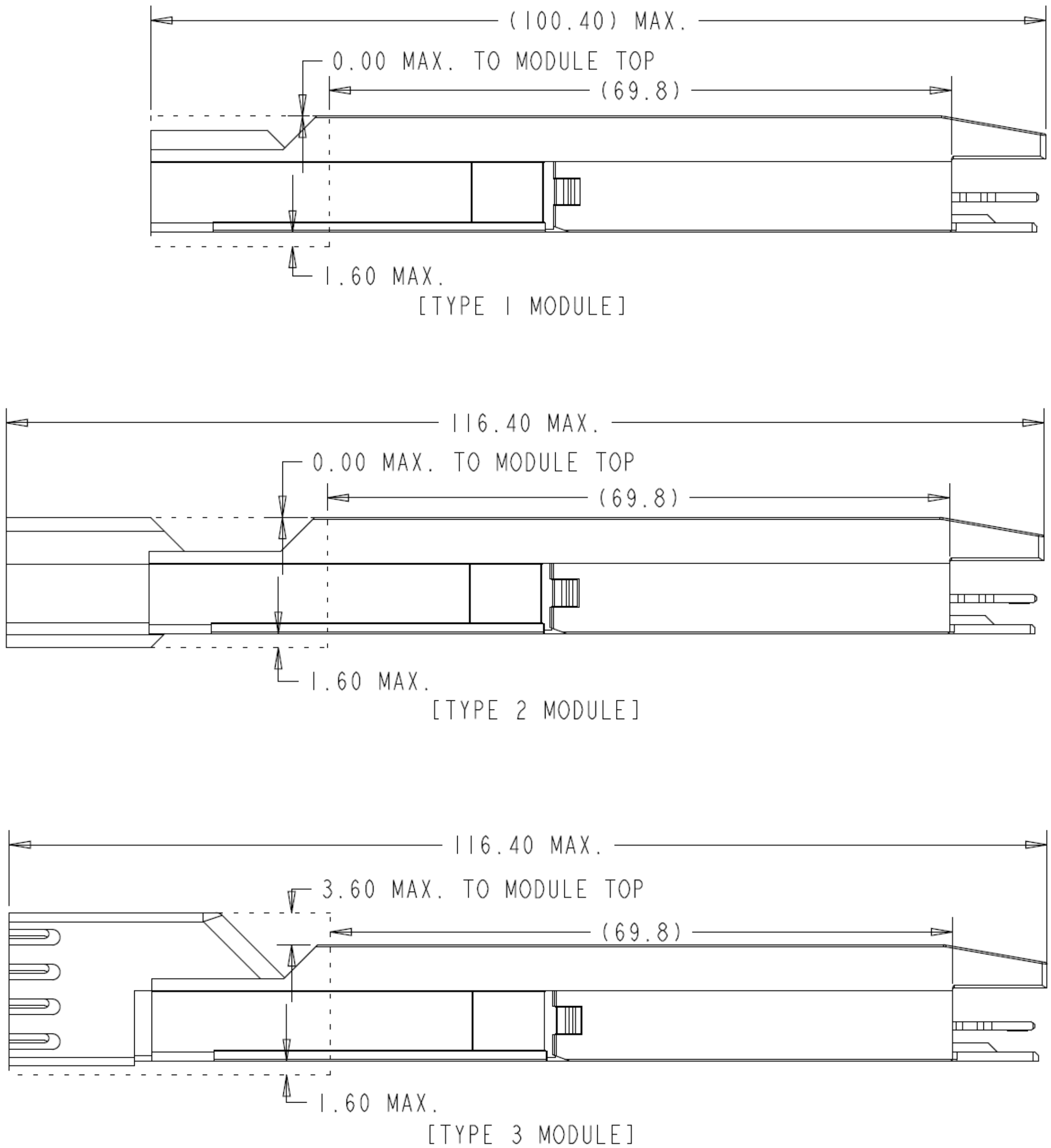


Figure 3-3: Size of module front, for Type 1, Type 2 and Type 3 OSFP

Figure 3-4 shows the recommended reference locations for the label. If the module has enough space outside of the cage, then the label can be placed as in the Figure 3-5 as well. While either location is allowed, the module shall have appropriate electrically conductive areas for ground contact. If the label is located inside the cage, then Figure 3-6 shows the recommended location. Also the edge of the label pocket should be designed so that it does not snagged during the module insertion, as shown in the same figure.

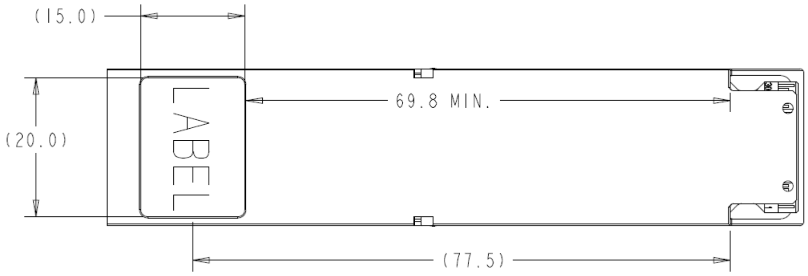


Figure 3-4: OSFP label, reference location

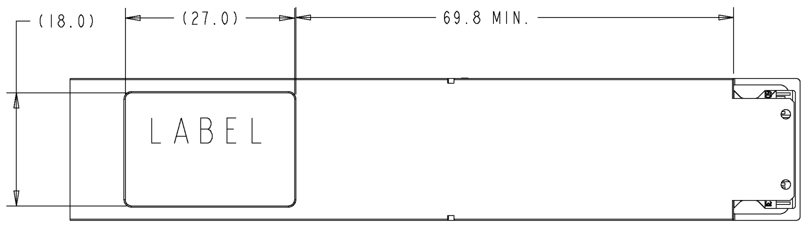


Figure 3-5: OSFP label, alternate reference location

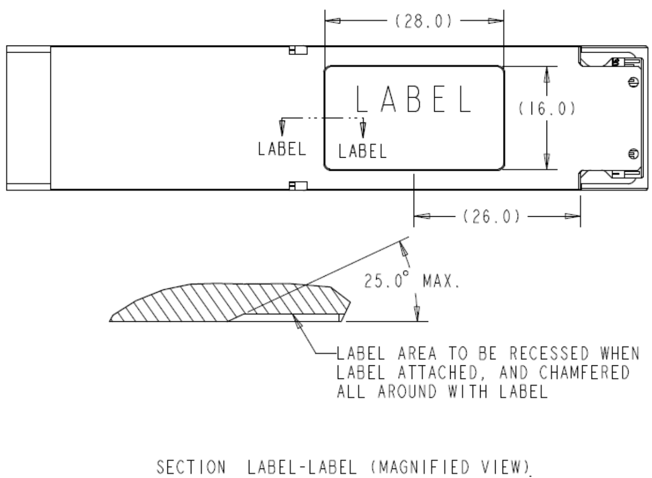


Figure 3-6: OSFP label, alternate reference location (inside the cage)

Figure 3-7 shows the corner radius of the module.

Figure 3-7: OSFP corner radius

3.2 OSFP, Back of the Module

To mate with an electrical connector located in a cage, an OSFP module shall have a protruded printed circuit board with contact pads. A structure in the back of the module serves as a guard to protect the PCB and gives lead-in when the module is being inserted to the cage. Figure 3-8 through Figure 3-14 show the dimensional requirements of the back of the module, including the shape of the housing, connector mating area, forward stop, ventilation holes, and the location of the signal pads.

Figure 3-10 shows the location of the forward stop, which consisting of the left and right vertical side walls of the bottom case of the module. These walls interact with features in the connector cage to stop the module when it is fully inserted.

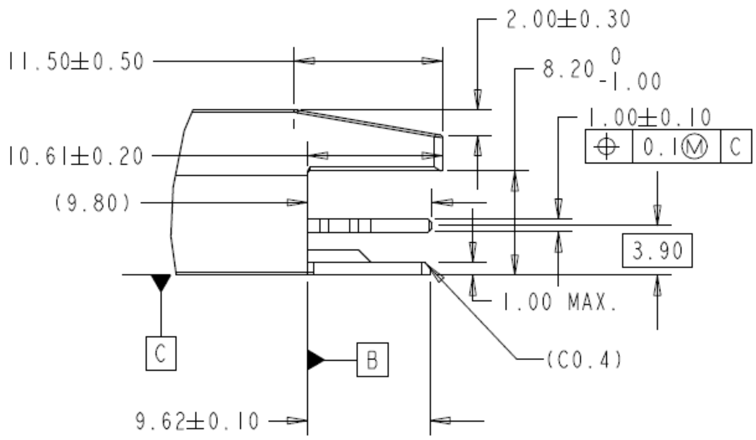


Figure 3-8: OSFP back, side view

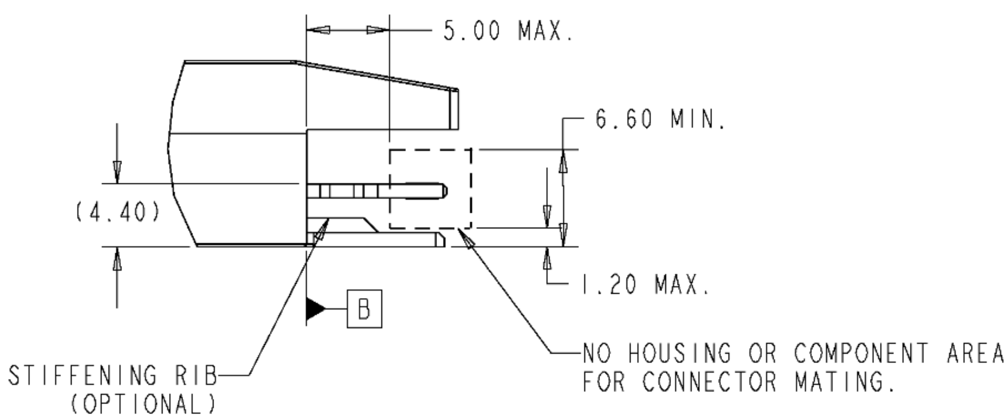


Figure 3-9: OSFP, back, side view, no component area

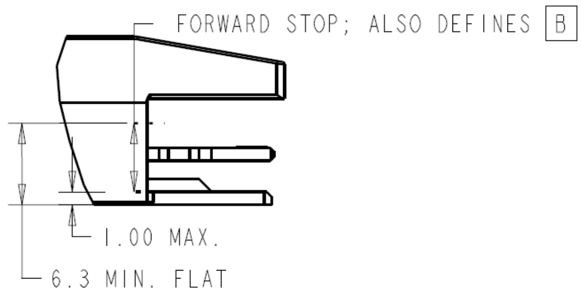


Figure 3-10: OSFP, back, side view, location of the forward stop

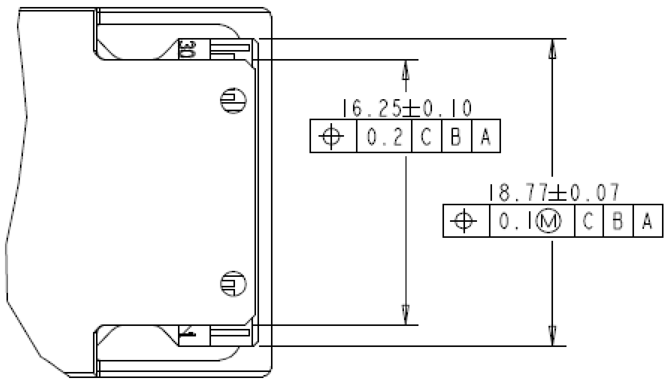


Figure 3-11: OSFP, back, bottom view

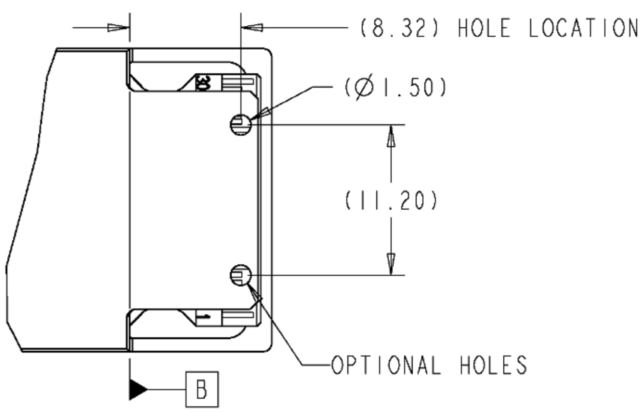


Figure 3-12: OSFP, back, bottom view, optional signal pad inspection holes

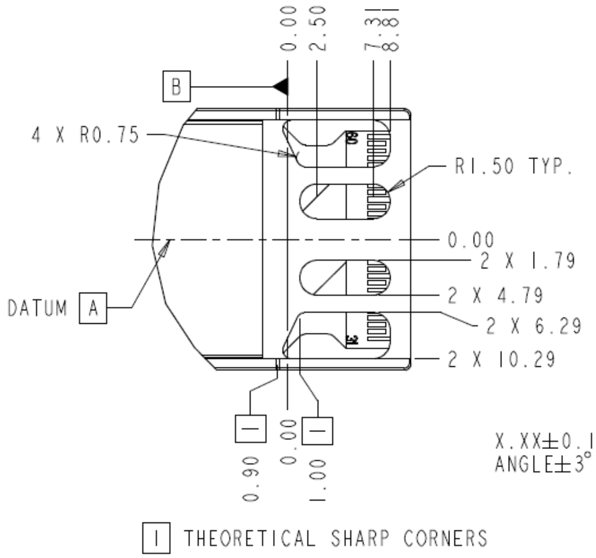


Figure 3-13: OSFP, back, top view: dimension for ventilation holes

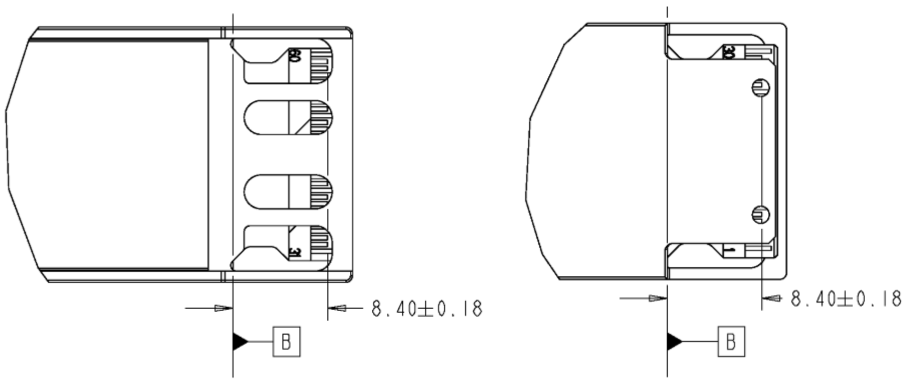


Figure 3-14: OSFP, signal pad location relative to module (left: top view, right: bottom view)

3.3 Heat Sink, Closed Top

To dissipate heat, the module allows for airflow along its length. Figure 3-15 shows the requirements for the heat sink location to avoid collision with the keying feature in the cage, and also ensure proper contact with ground and an optional thermal interface. Refer to Figure 5-11 for details of the keying feature located in the cage.

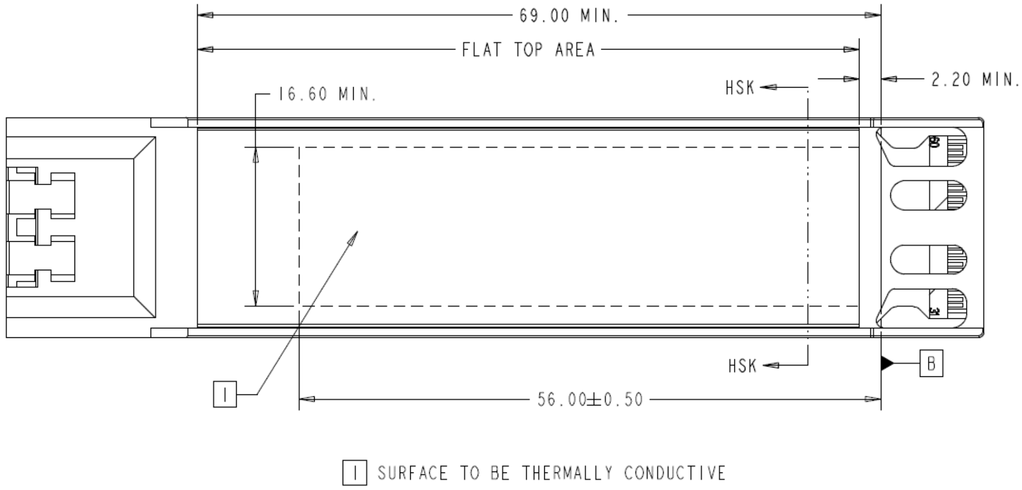


Figure 3-15: Heat sink, top view

The thermally conductive area in Figure 3-15 should have surface flatness and roughness as specified in Table 3-2. The area may be in contact with the riding heatsink, which depicted in the section 5.5.

Table 3-2: Surface flatness and roughness for the thermally conductive area

Module Power (Max.)	Surface Flatness	Surface Roughness
N/A	0.12mm or better	Ra 1.6µm or better
Recommended for modules rated for more than 20W (Optional)	0.075mm or better	Ra 0.8µm or better

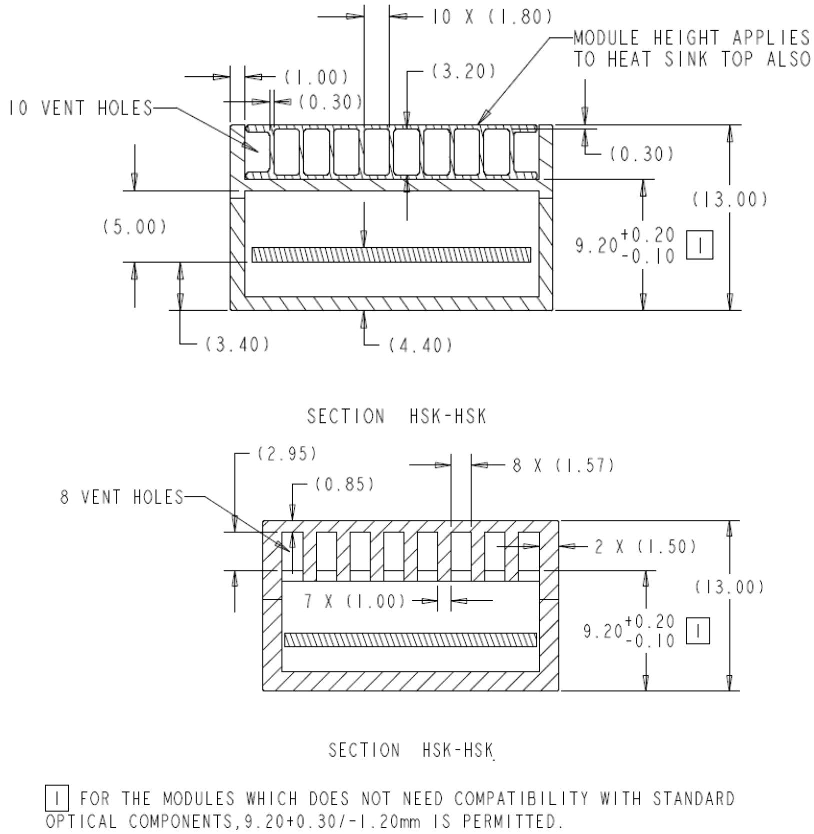


Figure 3-16: Examples of heat sink design (See Figure 3-15 for cross-section location)

Figure 3-16 presents two examples of heat sink design. Either may be considered for use. Alternate designs differing from the examples presented may also be used, but any heat sink design shall allow for sufficient airflow as defined in section 11.2.

As shown in Figure 3-17, the top trailing edge of the closed top heatsink shall have a minimum edge break to avoid riding heatsink damage.

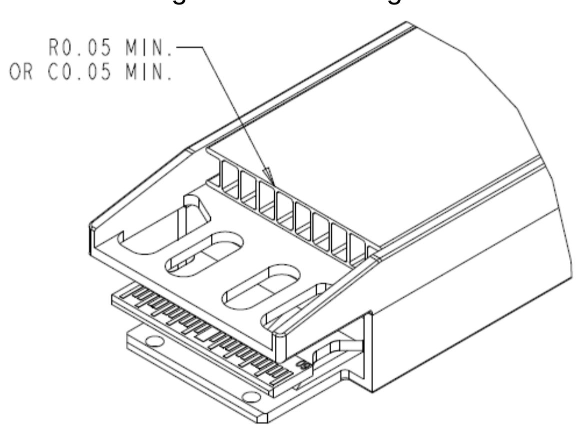


Figure 3-17: Flat top heatsink details, rear of plug

3.4 Heat Sink, Open Top

Modules which have a non-closed top, i.e. open top, are allowed only when the heat sink fins are designed to meet the dimensional requirements outlined in Figure 3-18 through Figure 3-20. Doing so prevents EMI finger damage ensures proper EMI shielding. The height and length of the heat sink may differ from the reference height presented, but shall still allow sufficient airflow as defined in section 11.2.

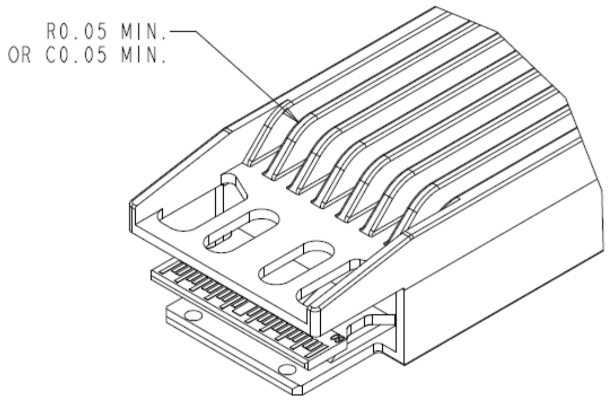


Figure 3-18: Open top heat sink (Isometric view)

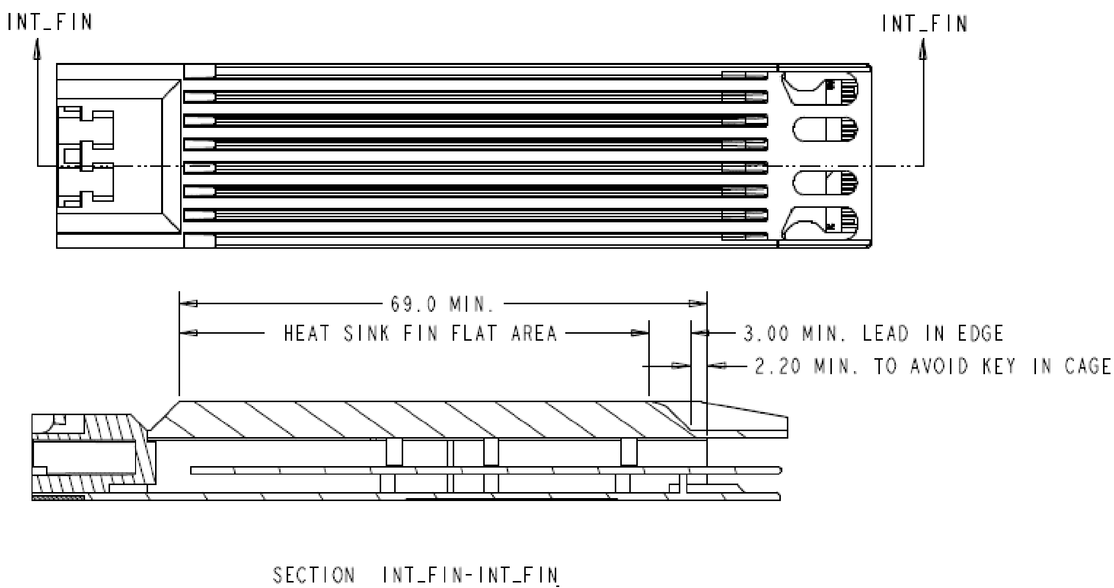


Figure 3-19: Heat sink location

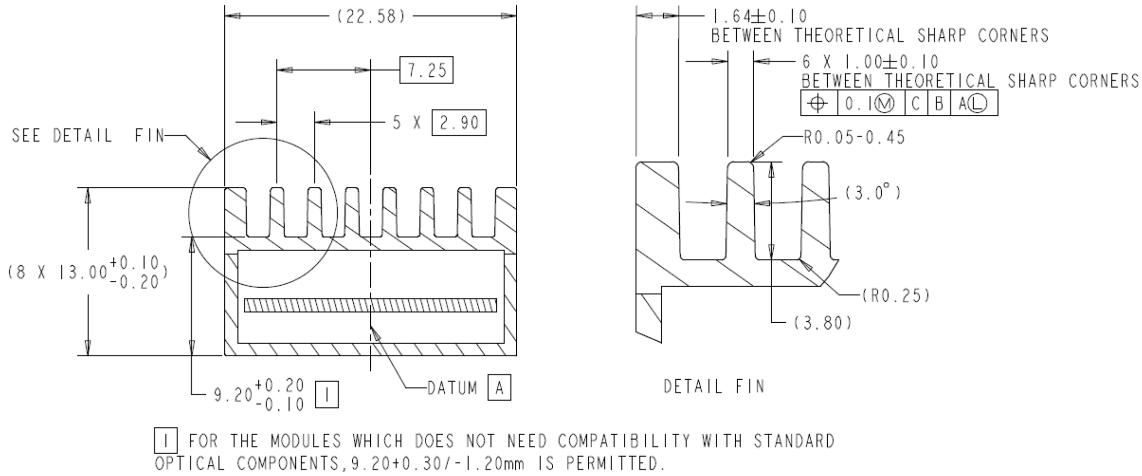


Figure 3-20: Heat sink fin pitch

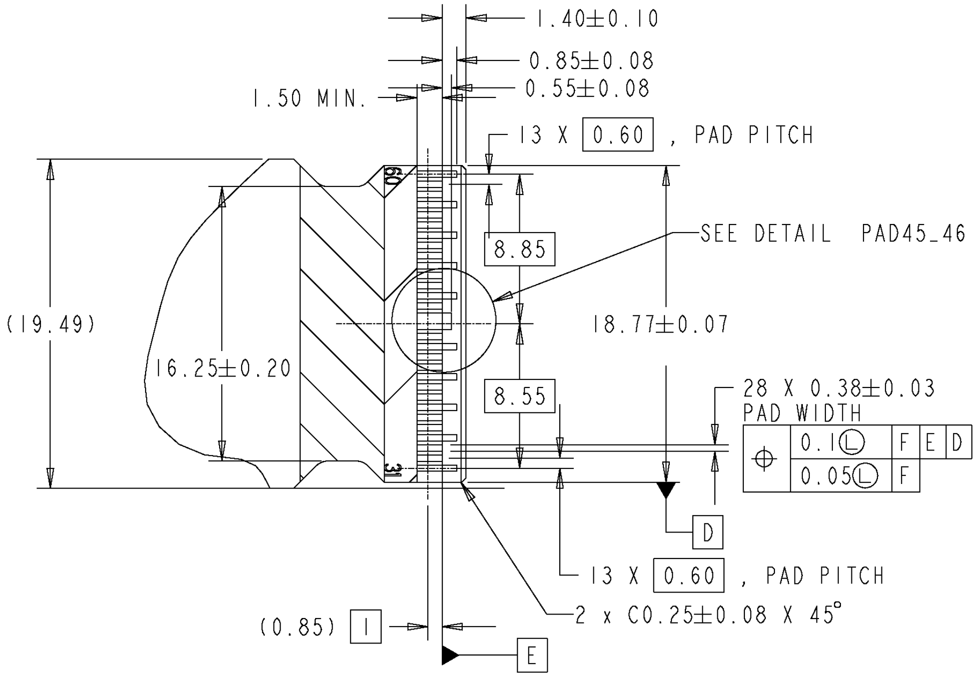
The top and bottom internal EMI fingers are specified per this fin pitch, as depicted in Figure 5-8. It is possible to add airflow passages to the bottom of the module with this fin pitch for thermal management of high-power modules.

3.5 Card-edge Design (Module Electrical Interface)

The OSFP module contains a PCB with contact pads (i.e., module PC board; paddle card) that mate with a connector as specified in section 5.10 of this document. Critical dimensions for the contact pads are shown in Figure 3-21 through Figure 3-23. The contact pads on the PCB are designed for sequential/chronological mating during module insertion as follows:

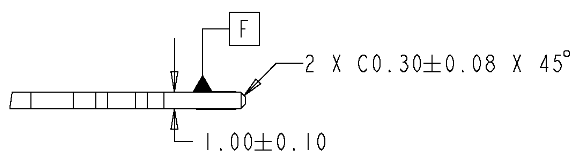
- First to mate: ground contacts
- Second to mate: power contacts
- Third to mate: signal contacts

During module removal, contact disconnects happen in reverse order of the above, e.g., signal contacts de-mate first.

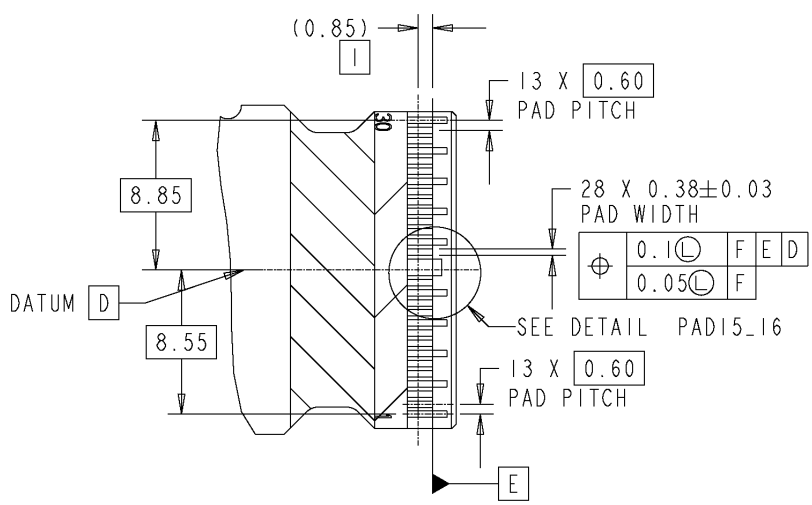


I NOMINAL CONTACT POINT WHEN THE MODULE IS FULLY PUSHED IN

TOP VIEW



SIDE VIEW



BOTTOM VIEW

Figure 3-21: OSFP module pc board (card-edge)

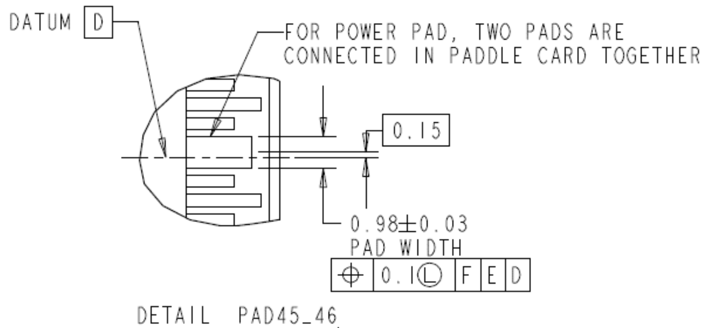


Figure 3-22: OSFP card-edge, detail of power pad (pads 45/46)

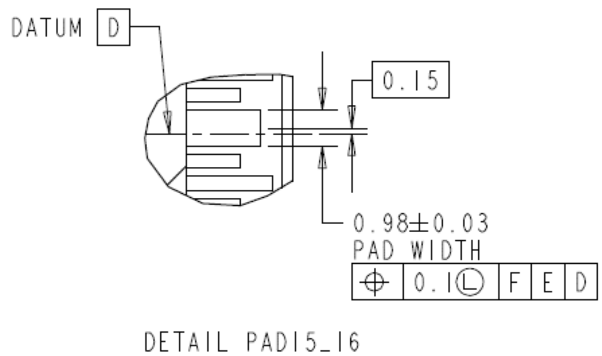


Figure 3-23: OSFP card-edge, detail of power pad (pads 15/16)

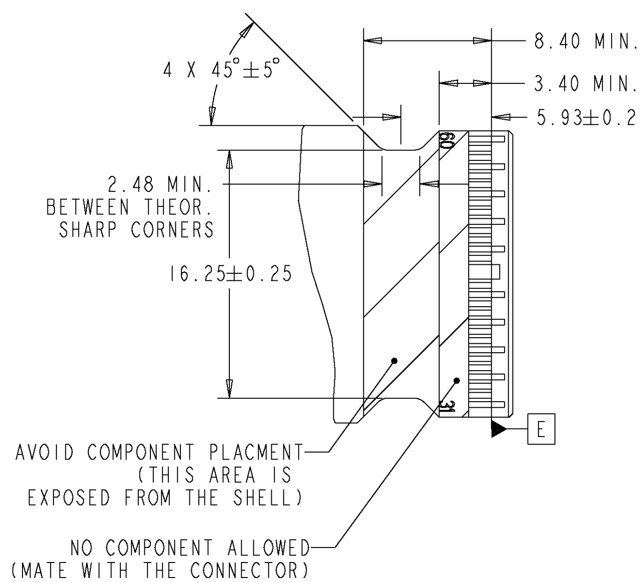


Figure 3-24: Keepout area and neck shape for OSFP

Figure 3-24 shows the keepout area of the paddle card, which applies to both side of the PCB. Also, same figure shows the details of the neck shape (area narrowed down), which applies to the OSFP, which support up to 50G per lane.

For OSFP800, the neck shape (area narrowed down) is optional. See the paddle card shape and the keepout area for the OSFP800 as in the Figure 3-25.

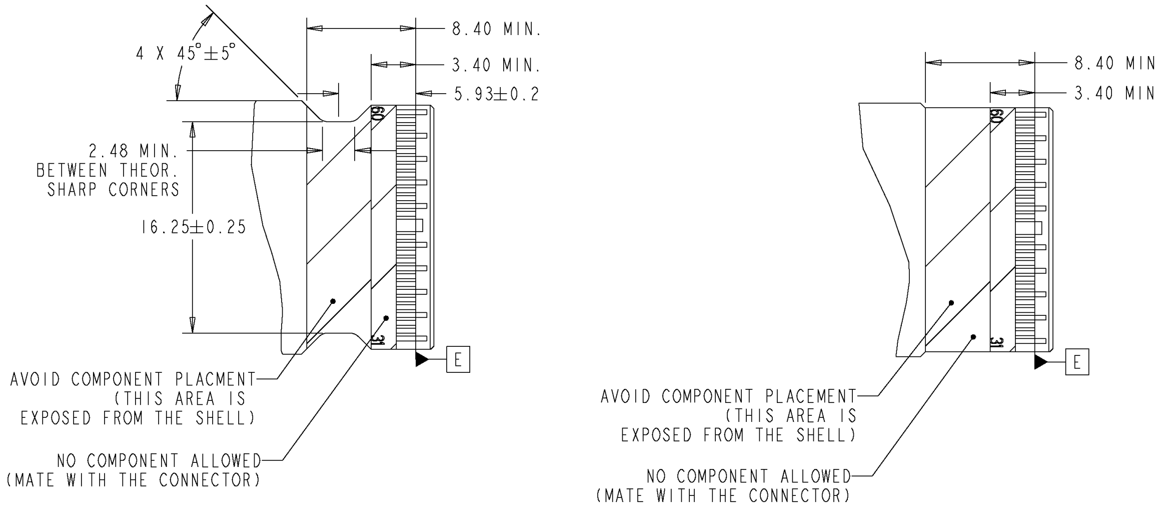


Figure 3-25: Keepout area and neck shapes for OSFP800 (both allowed)

3.6 Contact Pad Plating Requirements

The contact pad plating shall meet the durability requirements of section 10.1 and section 10.2. The recommended plating specification is a minimum of 0.762μm of gold over a minimum of 3.81μm of nickel. Other plating systems are allowed, provided they meet or exceed the requirements of sections 10.1 and 10.2.

3.7 Module Latch Feature

For latching, the module shall have latching pockets and a latch release mechanism at both sides, as shown in Figure 3-26 to Figure 3-29. Dimensional details of the cage flap can be found in Figure 5-20 and Figure 5-21.

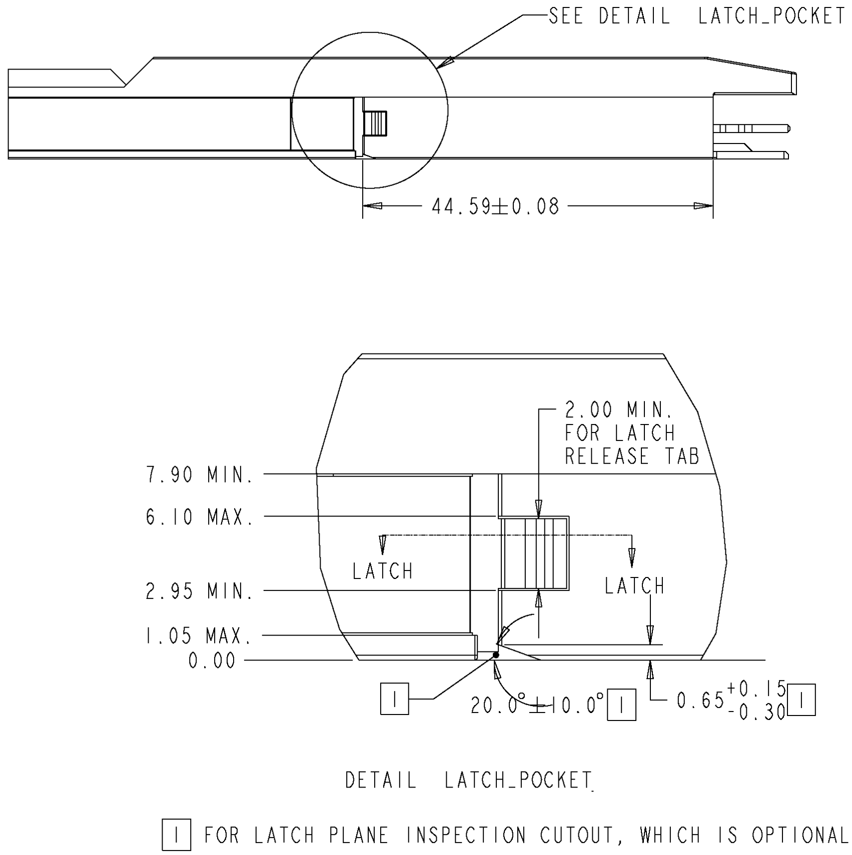


Figure 3-26: Latch pocket location

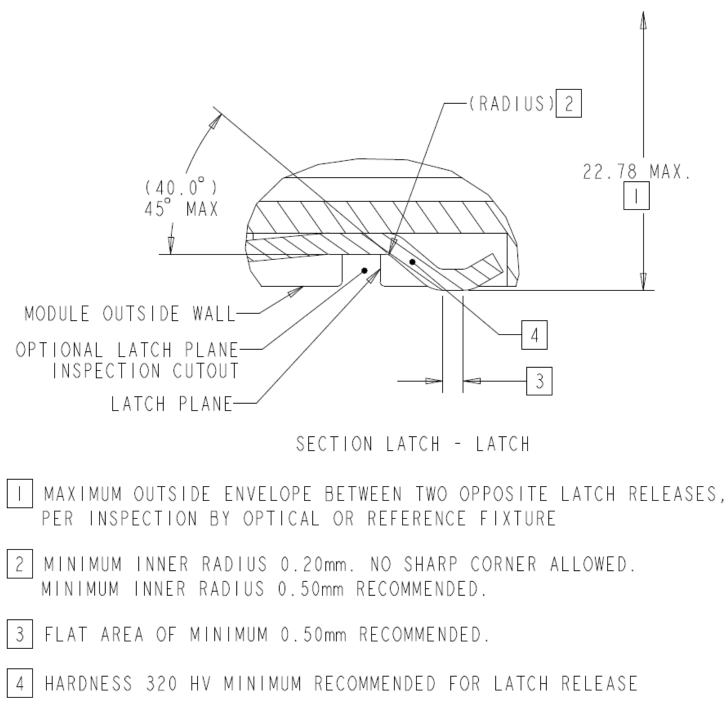


Figure 3-27: Latch release max width and latching pocket round

For the reference fixture mentioned in the Figure 3-27 note 1, see Appendix D.

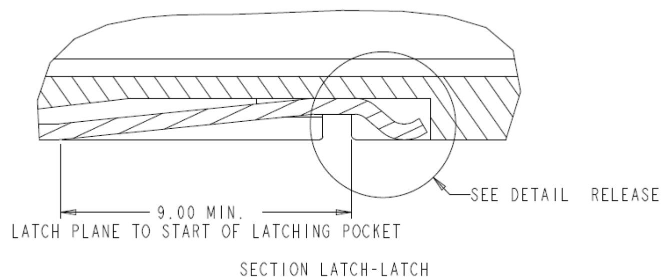


Figure 3-28: Latching pocket length

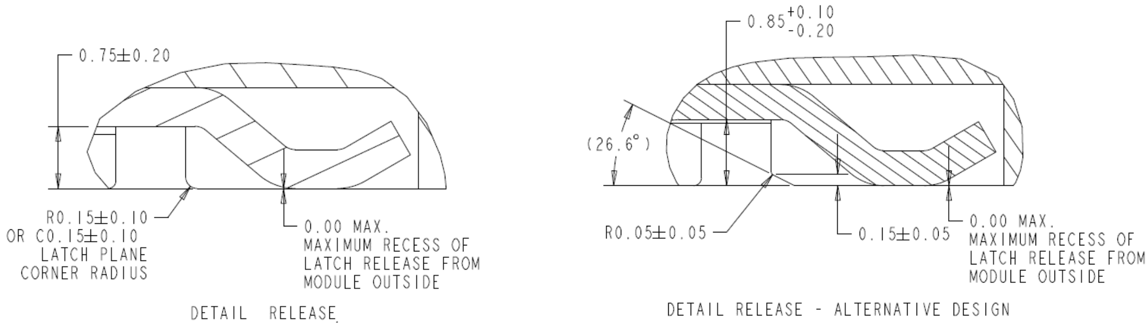


Figure 3-29: Latch plane corner radius and release details

In Figure 3-29, two reference designs are given. Different latch release designs are allowed, as long as reliable latch release can be achieved.

3.8 Module Color Code

The module shall adhere to a color code by application of color to its pull-tab or other appropriate method. The color code to be applied is given in Table 3-3.

Table 3-3: OSFP color code

Product Type	Example PMD	Color	Pantone Code (Recommended)
OSFP copper cables	400G/800G/1600G-CR8	Black	N/A
OSFP AOC Cables	400G/800G/1600G -AOC	Grey	422U
OSFP 850nm solutions	400G/800G/1600G -SR8, SR4.2	Beige	475U
OSFP 1310nm solutions for up to 500m	400G/800G/1600G DR4	Yellow	107U
OSFP 1310nm solutions for up to 2km	400G/800G/1600G FR4, FR8	Green	354C
OSFP 1310nm solutions for up to 10km	400G/800G/1600G LR8	Blue	300U
OSFP 1310nm solutions for up to 40km	400G/800G/1600G ER8	Red	1797U
OSFP 1550nm solutions for up to 80km	400G/800G/1600G ZR8	White	N/A

3.9 Touch Temperature

Module surfaces outside of the cage must comply with applicable touch temperature requirements. If the temperature of the module case will exceed applicable short-term touch limits, then a means to prevent contact with the case during the handling of the module shall be provided. Refer to UL 62368-1 and NEBS GR-63.

4 OSFP1600, Module Card Edge and Latch Specification

This section describes the amended mechanical specification to the section 3, which applies to the OSFP1600 modules. OSFP or OSFP800 may use the specification in this section. Specification in the section 4 should be applied as a whole, not partially applied.

Table 4 shows the mechanical cross-compatibility between the cages and modules of OSFP/OSFP800 and OSFP1600. Besides the speed and throughput differences, there are subtle differences in the mechanical and tolerance specifications between OSFP/OSFP800 and OSFP1600. OSFP1600 modules can be plugged into and recognized by the OSFP/OSFP800 port. However, such a use case is not advisable as the module cannot operate at its originally designed maximum speed, and the electrical contact in the paddle card may not be guaranteed under worst case tolerance. Meanwhile, OSFP/OSFP800 will perform as the module designed in the OSFP1600 port.

Table 4. Compatibility of OSFP/OSFP800 and OSFP1600

	OSFP or OSFP800 Module	**OSFP1600 Module**
OSFP or OSFP800 Port (Connector/cage)	Supported use case	Module can be plugged and powered with reduced mechanical reliability; Use case not advisable
OSFP1600 Port (Connector/cage)	Supported backward compatibility (Function per OSFP/OSFP800 module)	Supported use case

4.1 Forward Stop of the Module to Leading Edge of the Signal Pad

Figure 4-1 replaces Figure 3-14, bringing the leading edge of the signal pad closer to the positive stop of the module.

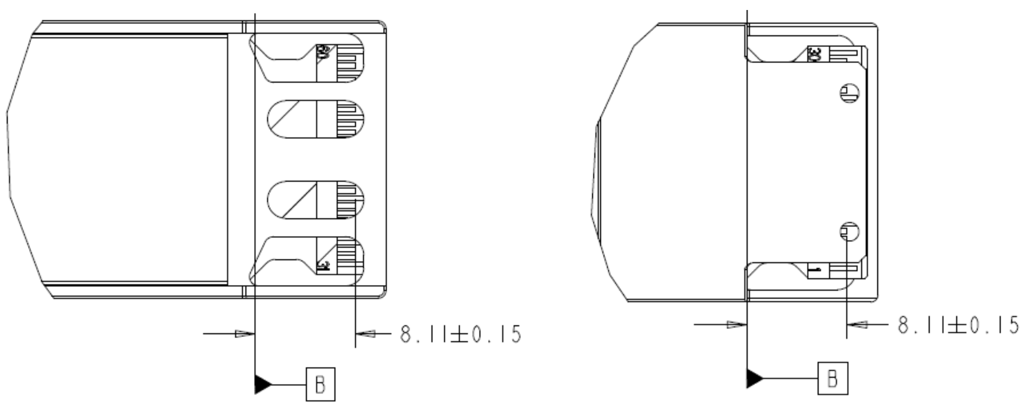


Figure 4-1: Signal pad location for OSFP1600 (left: top view, right: bottom view)

4.2 Card Edge Design, OSFP1600

Figure 4-2 and Figure 4-3 replaces Figure 3-21 for OSFP1600.

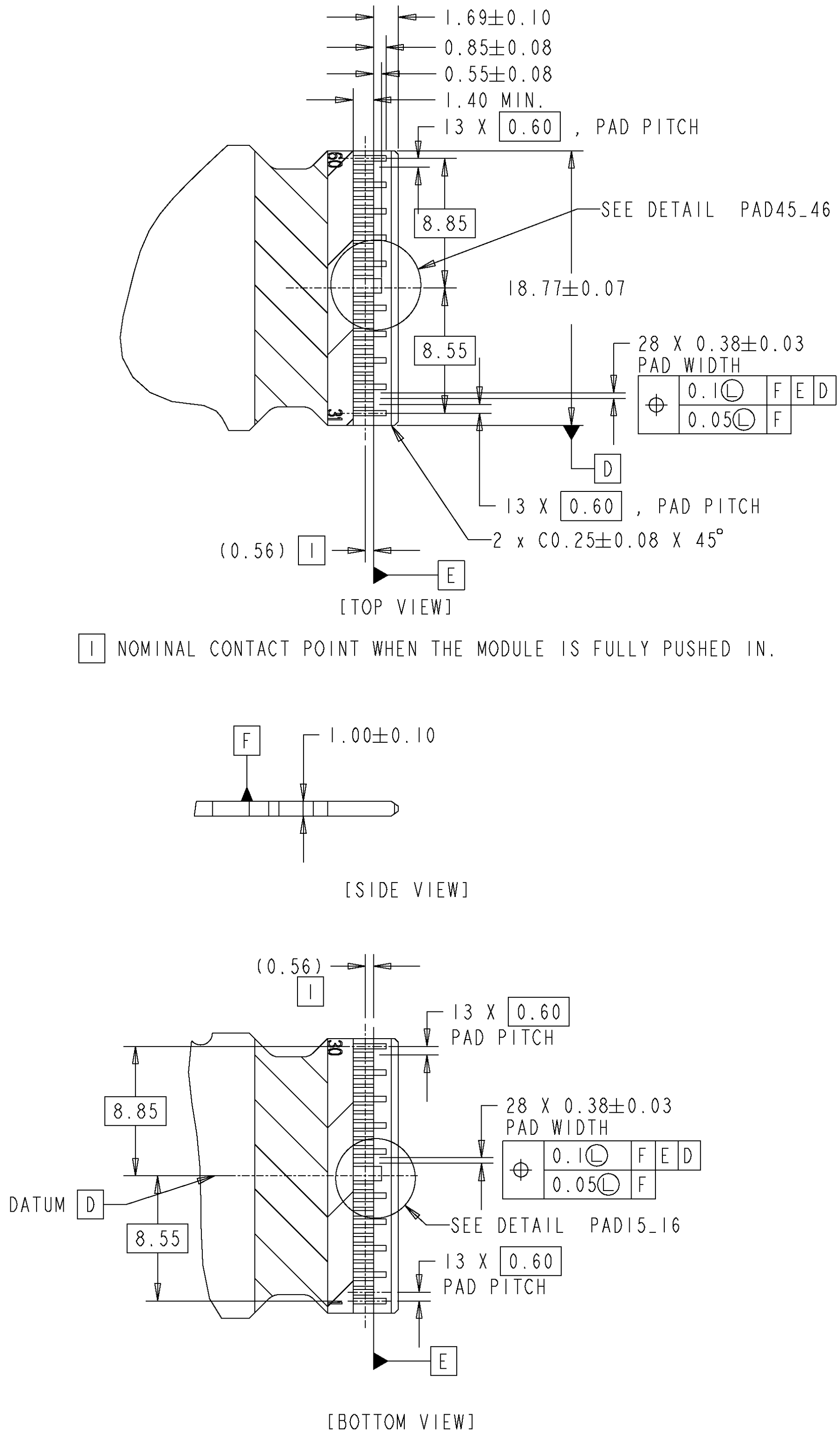


Figure 4-2: OSFP1600 module pc board (card-edge)

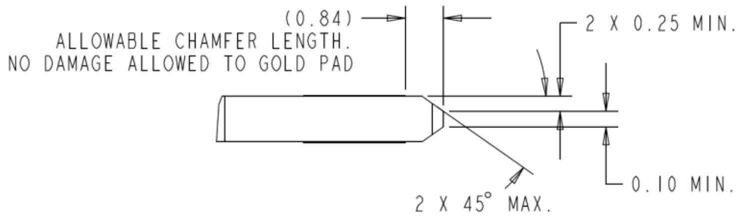


Figure 4-3: OSFP1600 module pc board chamfer (card-edge)

And Figure 4-3 shows the details of the lead-in chamfer. OSFP1600 paddle cards have shorter pad plates and allow a shallower lead-in chamfer.

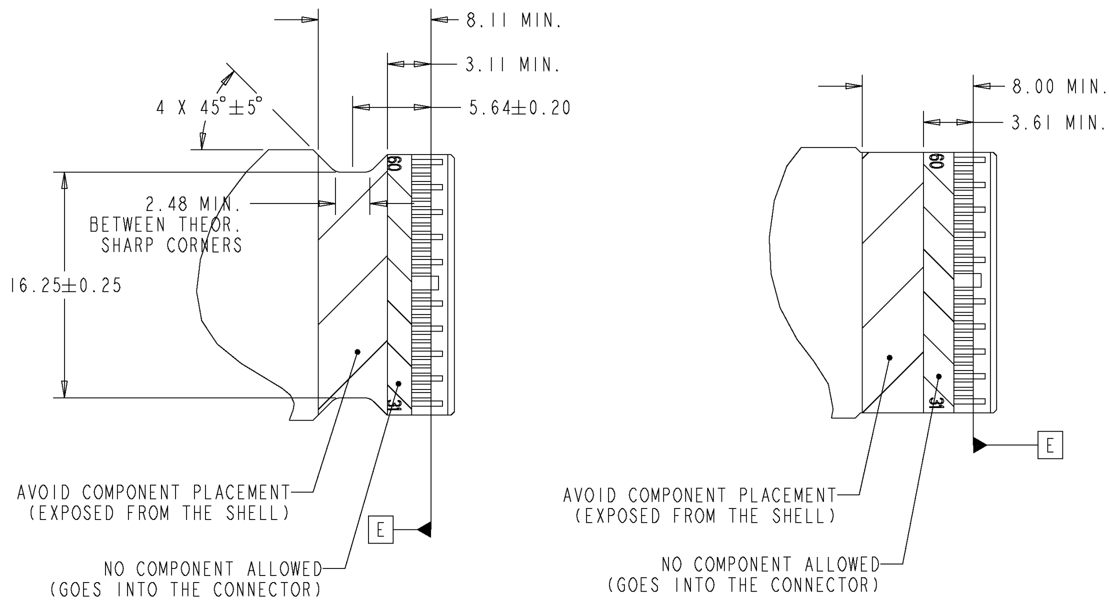


Figure 4-4: OSFP1600 module pc board (card-edge), neck area

For OSFP1600, the narrow neck of the PCB is optional, and either design in the Figure 4-4 can be used.

4.3 Module Latch Feature

This section replaces section 3.7. Figure 4-5 and Figure 4-6 shows that the latch location from the bottom of the module and the latch pocket length for OSFP1600 is identical to OSFP.

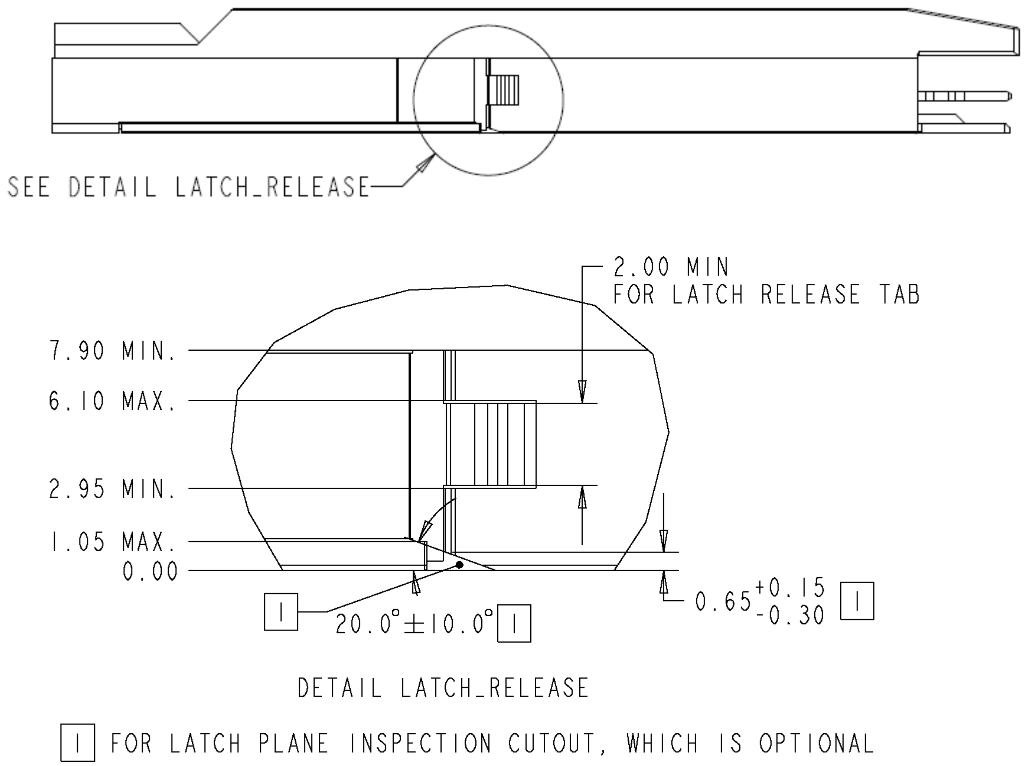


Figure 4-5: OSFP1600 module latch pocket location

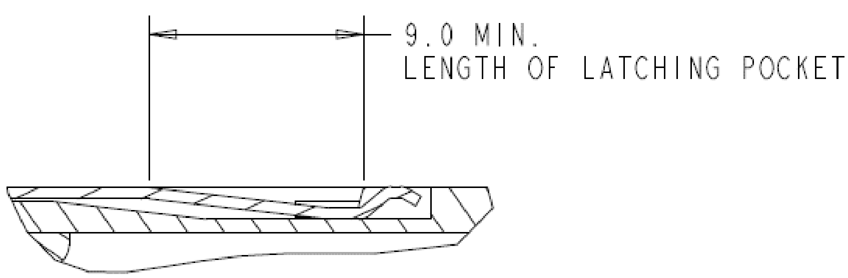


Figure 4-6: OSFP1600 module latch pocket length

As shown in Figure 4-7 and Figure 4-8, the latching pocket depth and latching wall angle is designed to minimize the module front-to-back clearance. The module label pocket is identical to OSFP, which is depicted in Figure 3-6.

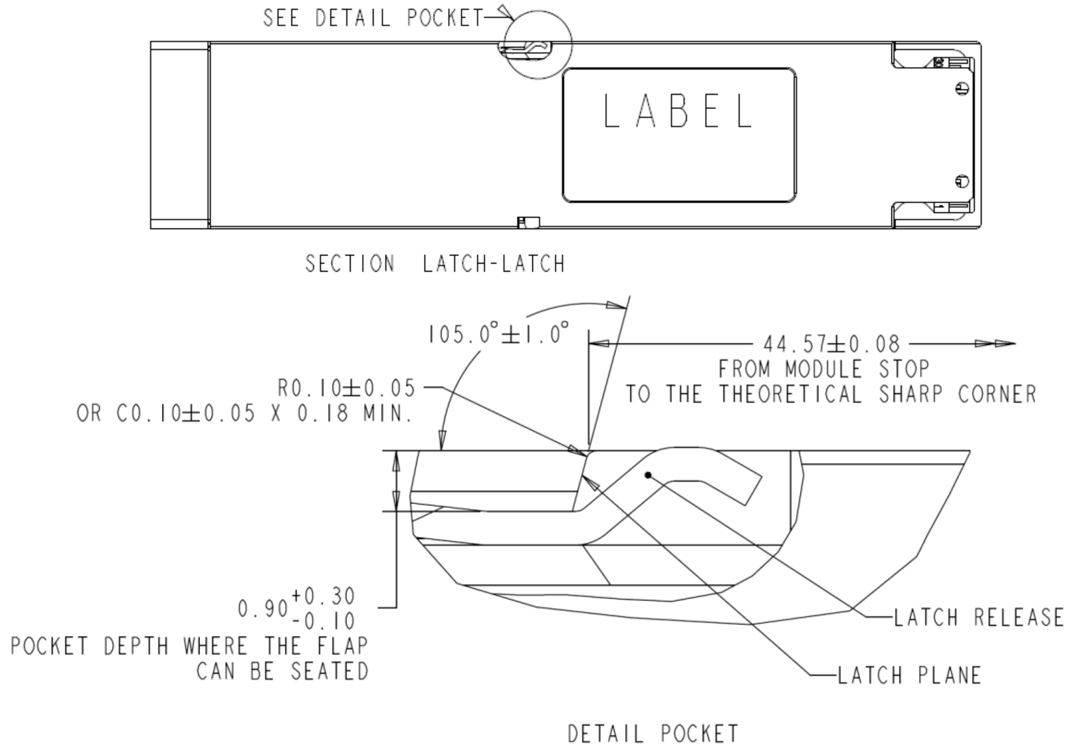


Figure 4-7: OSFP1600 module latch pocket depth and angle

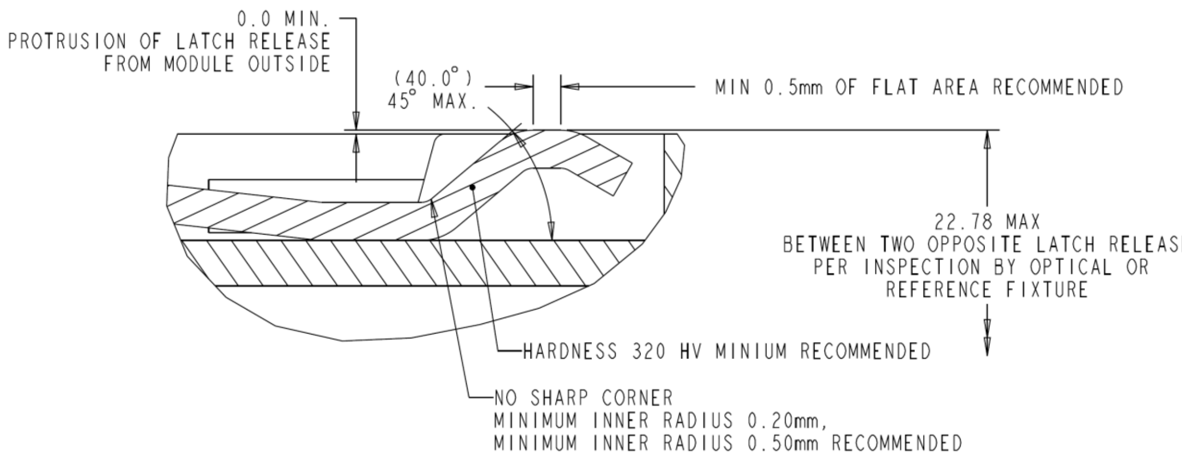


Figure 4-8: OSFP1600 module latch release details

For the reference fixture mentioned in the dimension 22.78mm in the Figure 4-8, see Appendix D.

5 Single Row Surface Mount Technology OSFP Connector and Its Cage: Mechanical Specification

In this section, the configuration of a single row Surface Mount Technology (SMT) connector and its cage for OSFP and OSFP800 are presented. For OSFP1600 SMT connector and cage, refer this section and section 6.

5.1 Overview

Figure 5-1 gives an overview of a 1x1 and 1x4 cage without modules installed. Figure 5-2 depicts a 1x1 cage with an OSFP module in the fully inserted position.

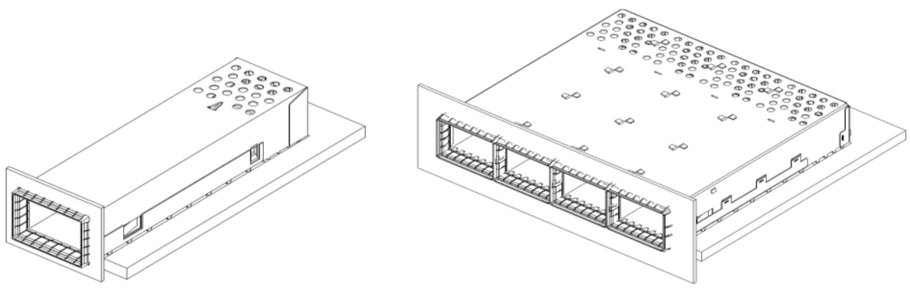


Figure 5-1: 1x1 and 1x4 cage, host PCB and panel

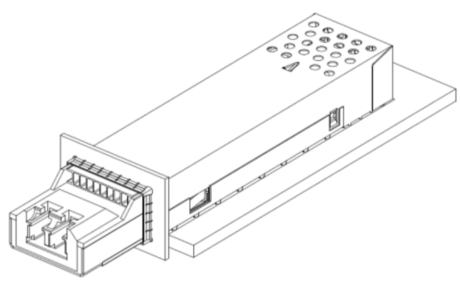


Figure 5-2: OSFP module in a 1x1 cage

In the cage and connector mechanical drawings included throughout this specification, the datum as defined in Table 5-1 shall apply. For datum of the module, see Table 3-1.

Table 5-1: Descriptions of the cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 5-3
H	Seating plane of Cage on host pc board	Figure 5-3
J	Width of inside of Cage	Figure 5-4
K	Connector guide post #1	Figure 5-6; Figure 5-25
L	Cage Pin #1	Figure 5-3
M	Top surface of host pc board. Defined by plated pads in OSFP1600	Figure 5-15; Figure 6-1
N	Host pc board through hole #1 to accept Connector guide post	Figure 5-15
P	Host pc board through hole #2 to accept Connector guide post	Figure 5-16
R	Host pc board through hole #1 to accept Cage Pin	Figure 5-16
S	Width of Connector	Figure 5-25
T	Front surface of Connector	Figure 5-25
U	Seating plane of Connector. Defined by the 4 standoffs in OSFP1600	Figure 5-25; Figure 6-6

5.2 Cage Dimensions and Positioning Pin

Figure 5-3 through Figure 5-5 show the cage datum, positioning pin, port size, and cage height. In addition, Figure 5-6 shows the nominal dimensions between the module and the cage when the module is fully inserted. Note that the compliant pins in the cage are placed to support belly-to-belly applications. For ganged cages, some compliant pins shall be shorter to support the belly-to-belly application properly. Figure 5-7 shows the length of the compliant pins for a 1x4 cage. Figure 5-18 shows the host PCB board layout for a 1x4 cage.

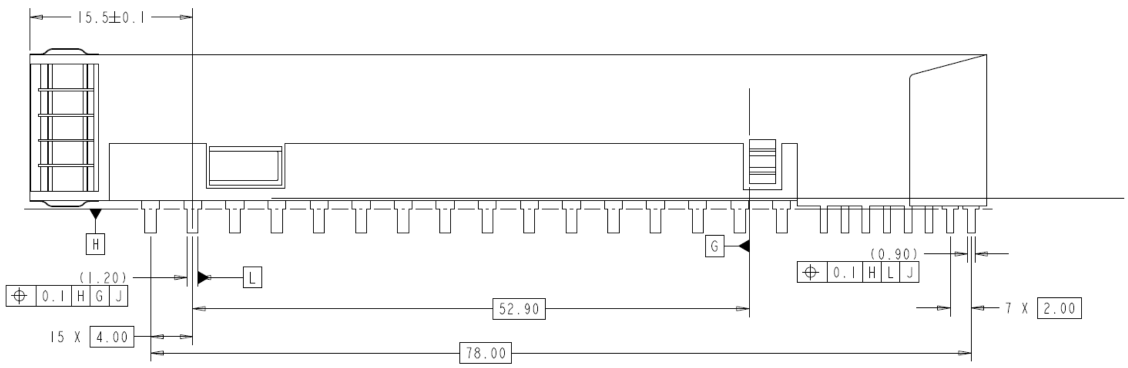


Figure 5-3: Cage positioning pins and forward stop

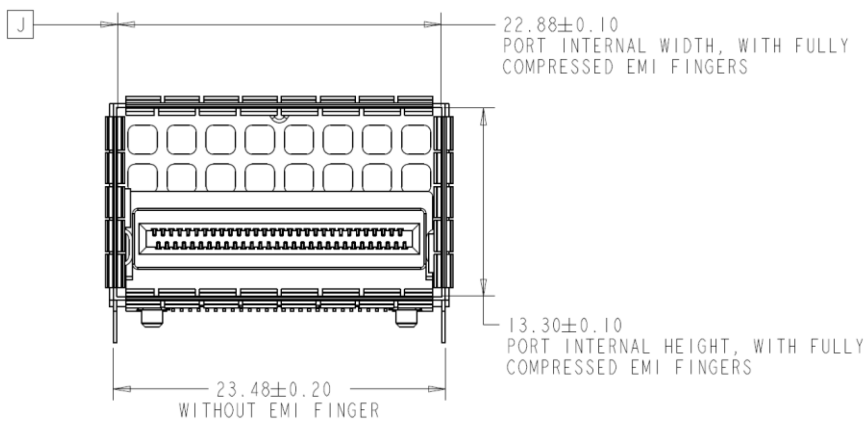


Figure 5-4: Port internal width and height

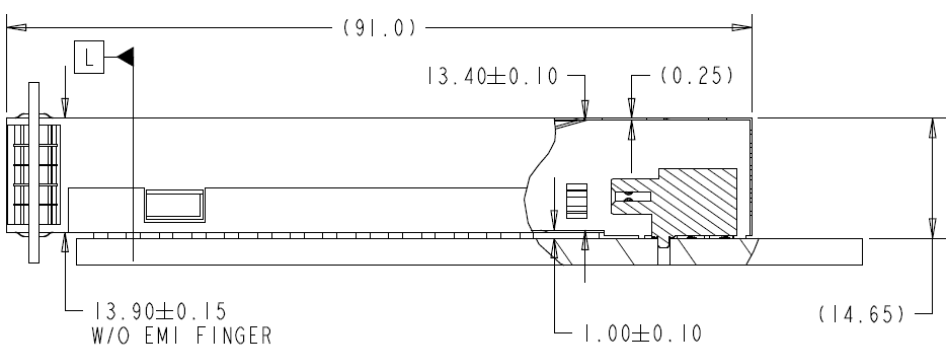


Figure 5-5: Side view of a 1x1 cage with vertical cage dimensions

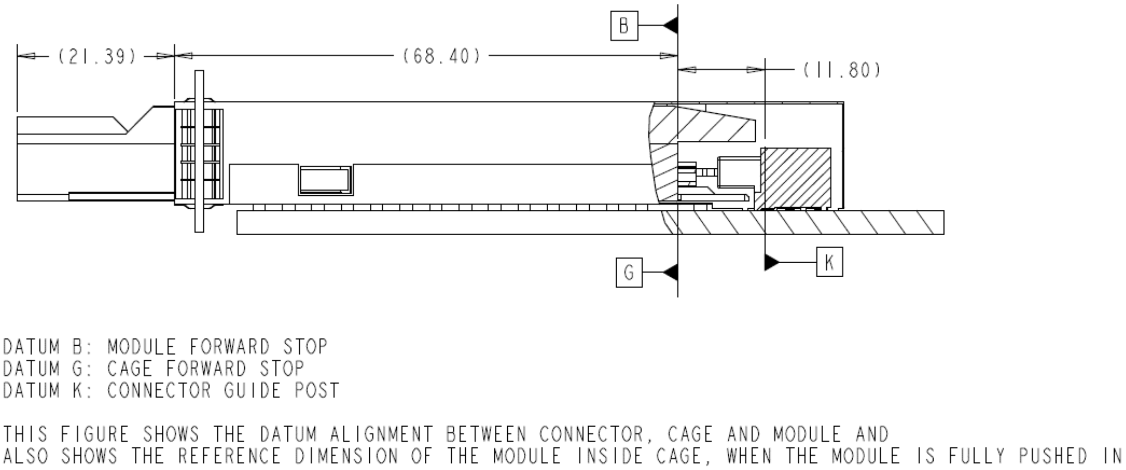


Figure 5-6: Side view of a 1x1 cage with axial reference dimensions

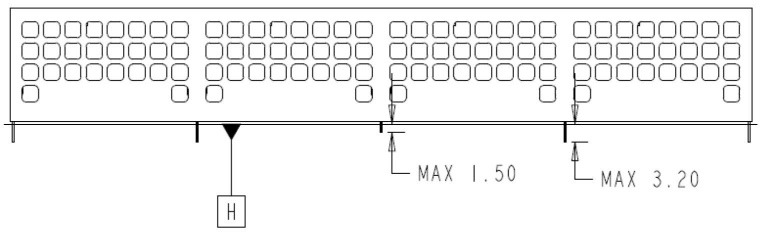


Figure 5-7: Length of the compliant pins into the board, for belly-to-belly application

5.3 EMI Finger Pitches

Figure 5-8 provides the EMI finger dimensions to be used for the internal side of top and bottom EMI fingers. These pitches are designed such that the OSFP module as described in section 3.4 is compatible. Fingers for the left, right, and outside of the cage shall be designed to ensure appropriate EMI shielding, but finger pitch is not specified. This EMI finger pitch specification shall be applied to the stacked SMT cage (section 7) and stacked press-fit cage (section 8).

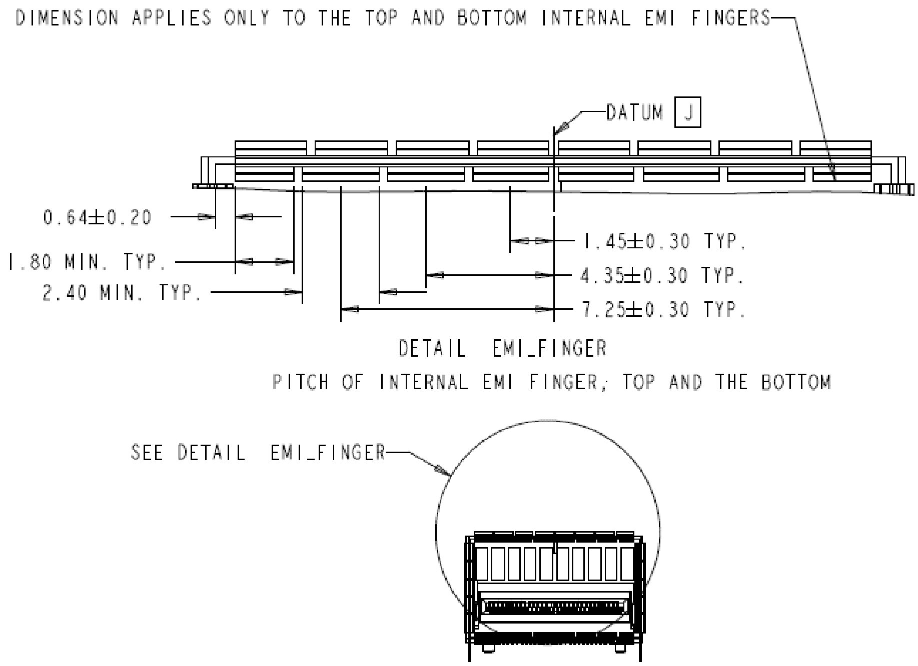


Figure 5-8: Internal EMI finger, top and bottom

5.4 Ventilation Hole, Key and Stop

Figure 5-9 shows the keying and forward stop features. The keying feature will prevent the module from being inserted upside down.

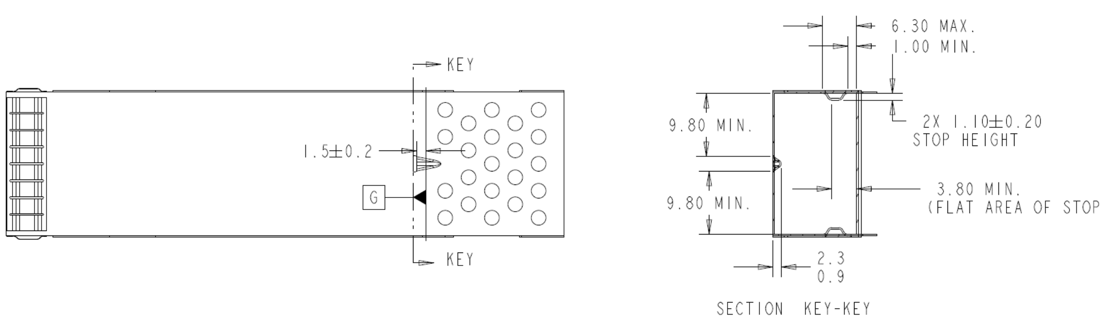


Figure 5-9: Key and stop

The cage should have ventilation holes to allow for airflow. Refer to Figure 5-10 and Figure 5-11 for examples of ventilation hole details. Other ventilation hole designs are permissible. Figure 5-12 shows ventilation hole on the bottom side of the cage, which is optional.

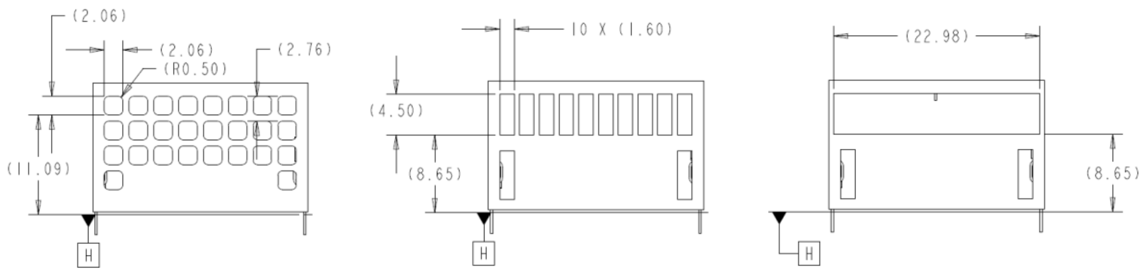


Figure 5-10: Rear ventilation holes, three example designs

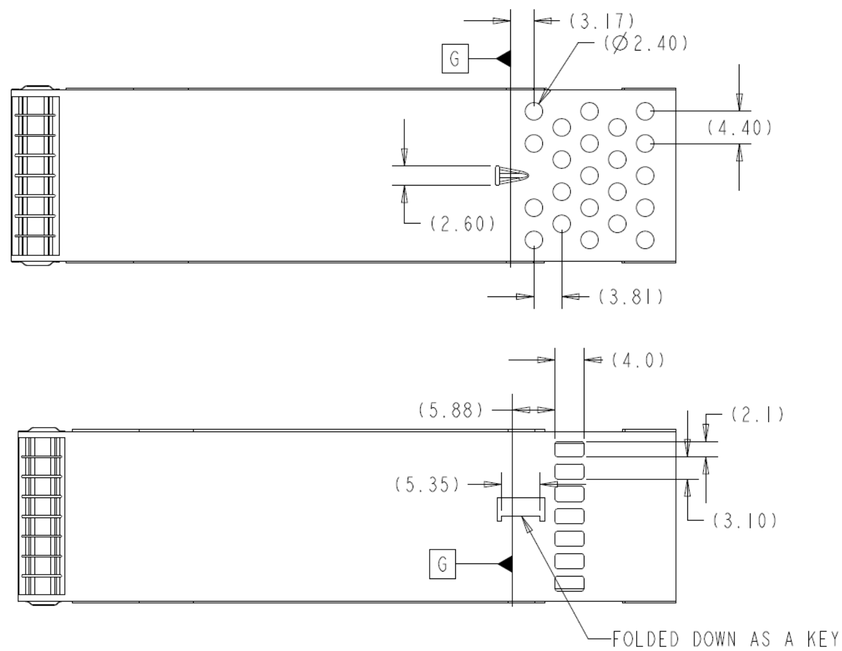


Figure 5-11: Top ventilation holes, two example designs

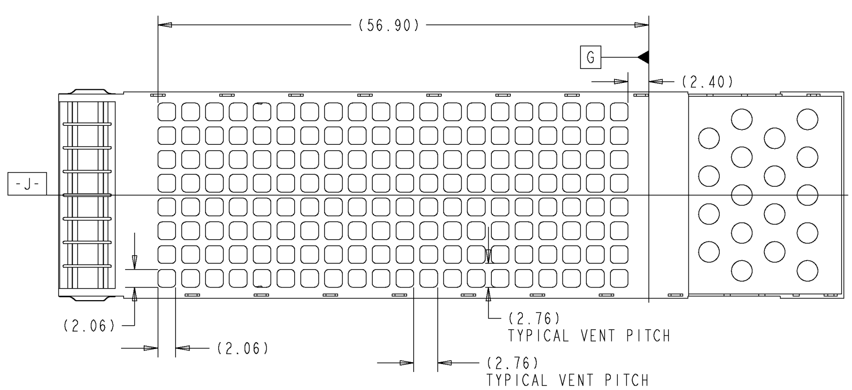


Figure 5-12: Bottom ventilation holes (Optional)

5.5 Extra Riding Heatsink

An OSFP cage may have an extra riding heatsink. Figure 5-13 shows the cutout size of the cage for the riding heatsink. Figure 5-14 shows the reference design of the leading edge of a riding heatsink. The down force which will be applied from the riding heat sink to an OSFP module should not exceed 36N.

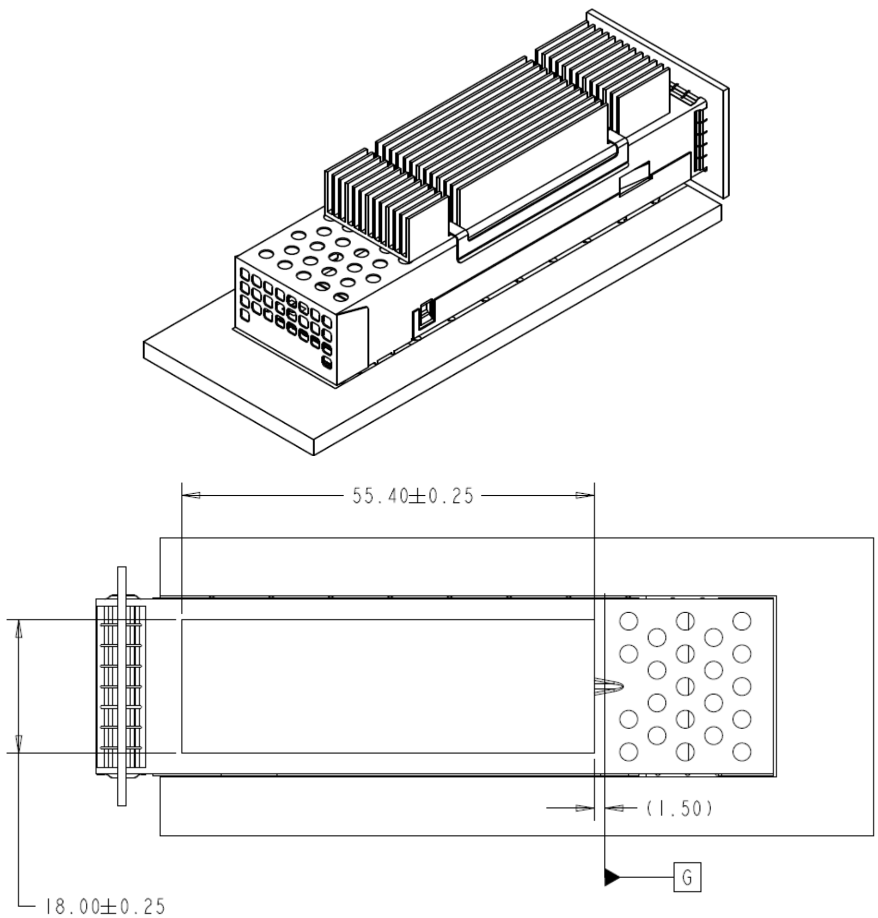


Figure 5-13: OSFP with a riding heatsink (above) and cutout on the cage (bottom)

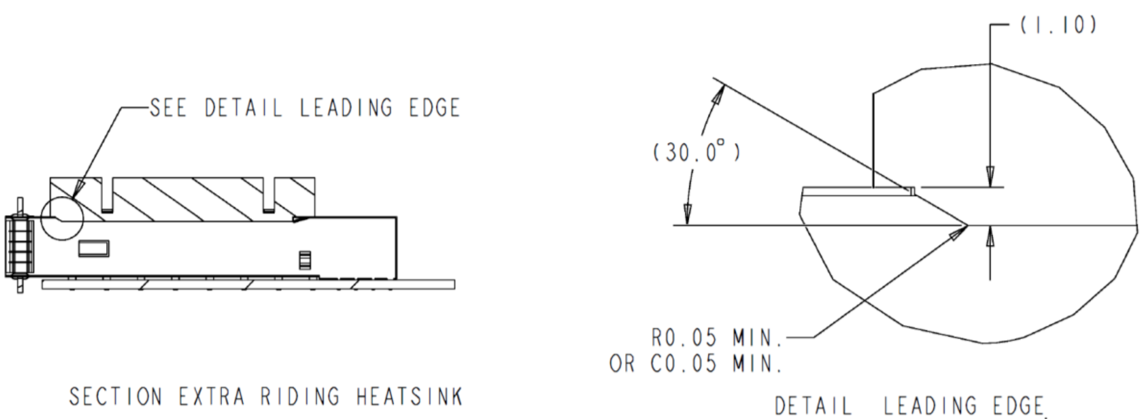


Figure 5-14: Heat sink leading edge, reference design

5.6 Host PCB Layout – 1x1 Cage

The host PCB layout pattern to accept a 1x1 cage is detailed in Figure 5-15 through Figure 5-17.

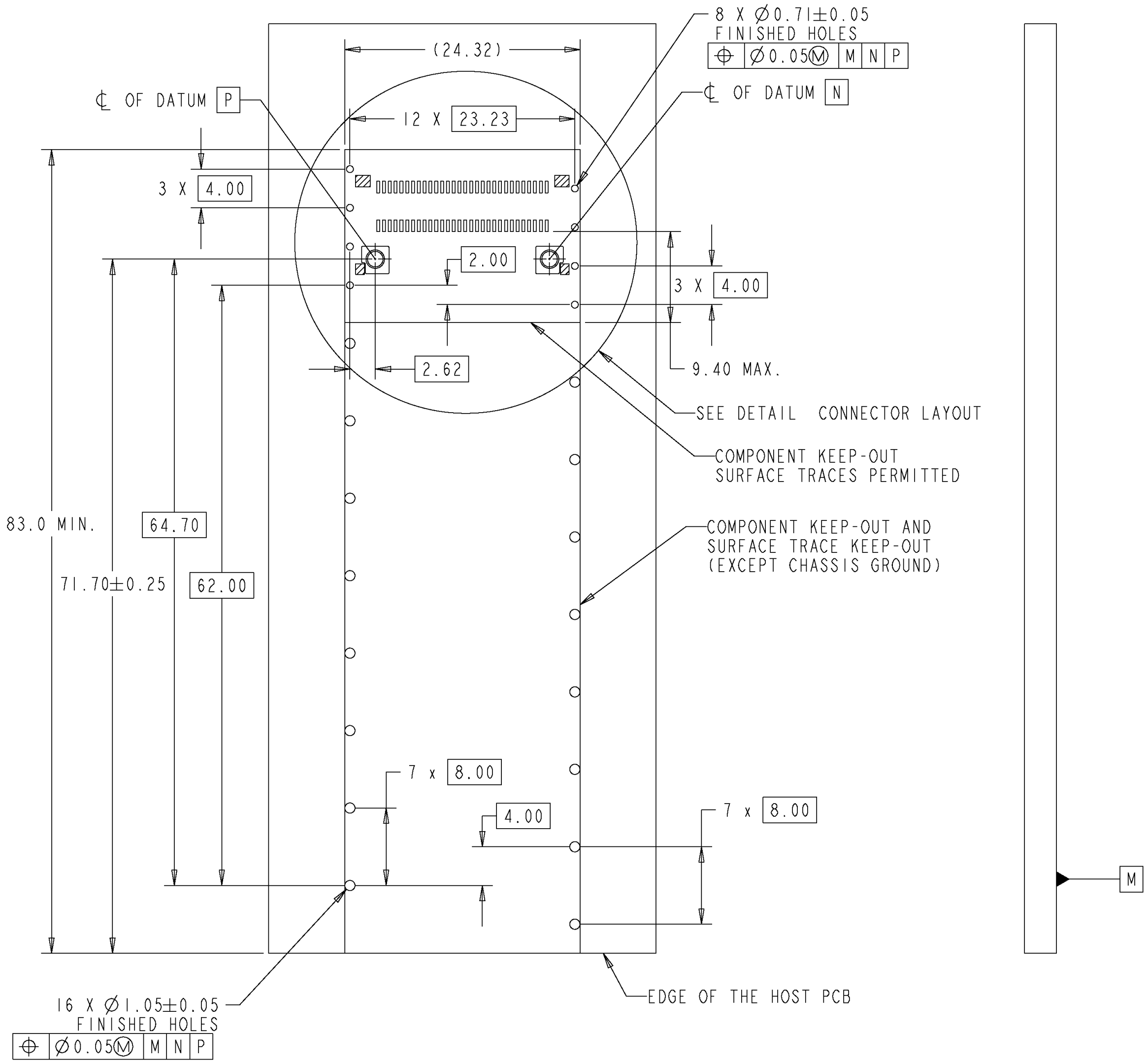


Figure 5-15: Host PCB layout for 1x1 cage

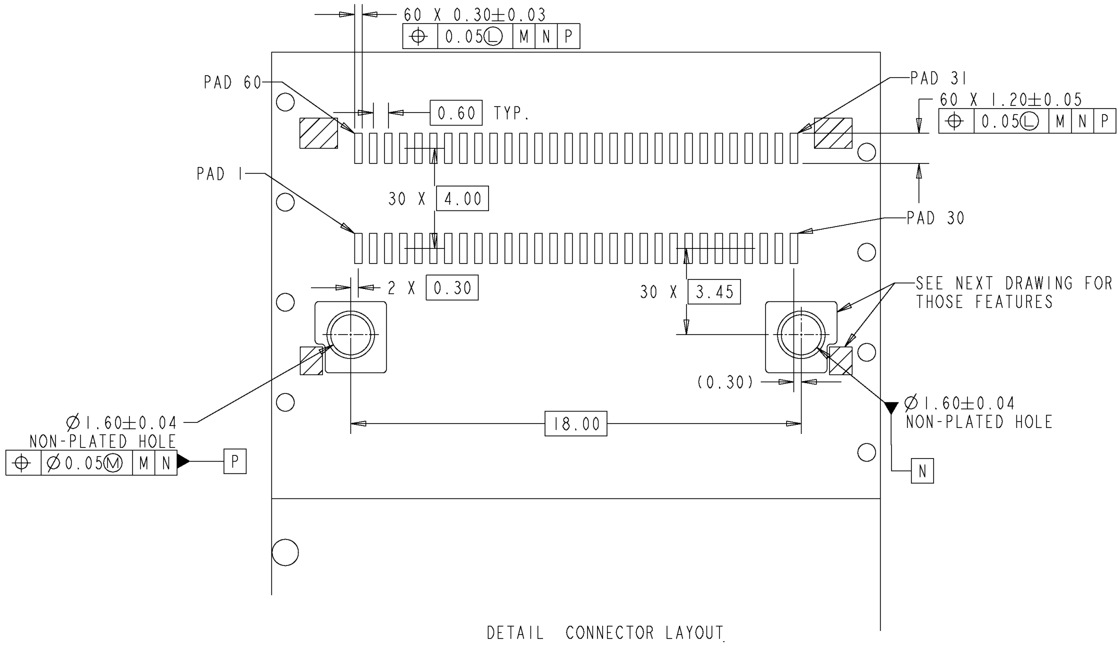


Figure 5-16: Host PCB layout, details

Figure 5-17 shows keepout areas and optional pads for solder rings. The solder rings are for SMT belly-to-belly applications, thus applying solder to the area is optional. The keepout areas are there in order to prevent interference with the connector in Figure 5-25. The keepout areas should be kept in the layout in all cases regardless of whether solder is applied to the optional solder ring area.

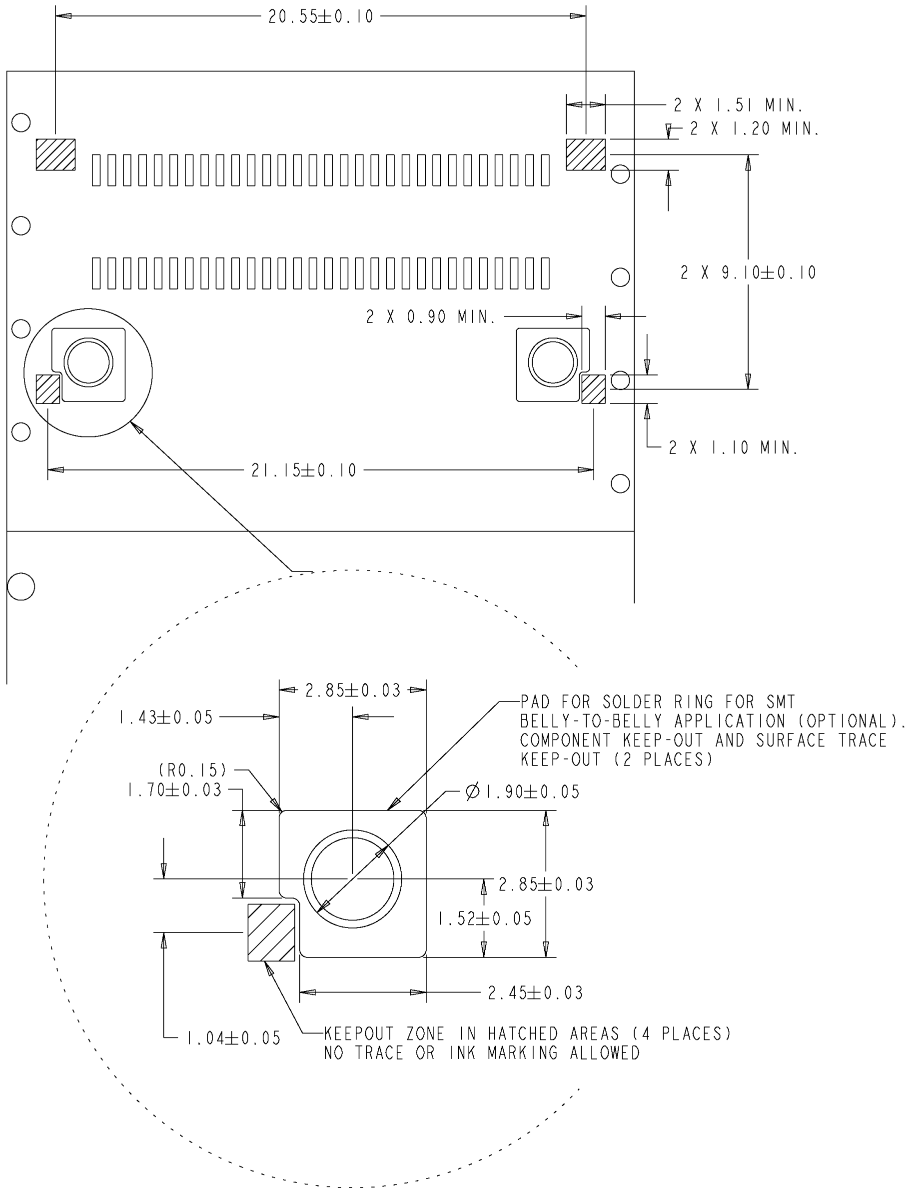


Figure 5-17: Pad for solder ring (for belly-to-belly application)

5.7 Host PCB Layout – 1x4 Cage

For a 1x4 cage, the host PCB layout shall have a 23.23mm horizontal pitch from cage-to-cage as in Figure 5-18.

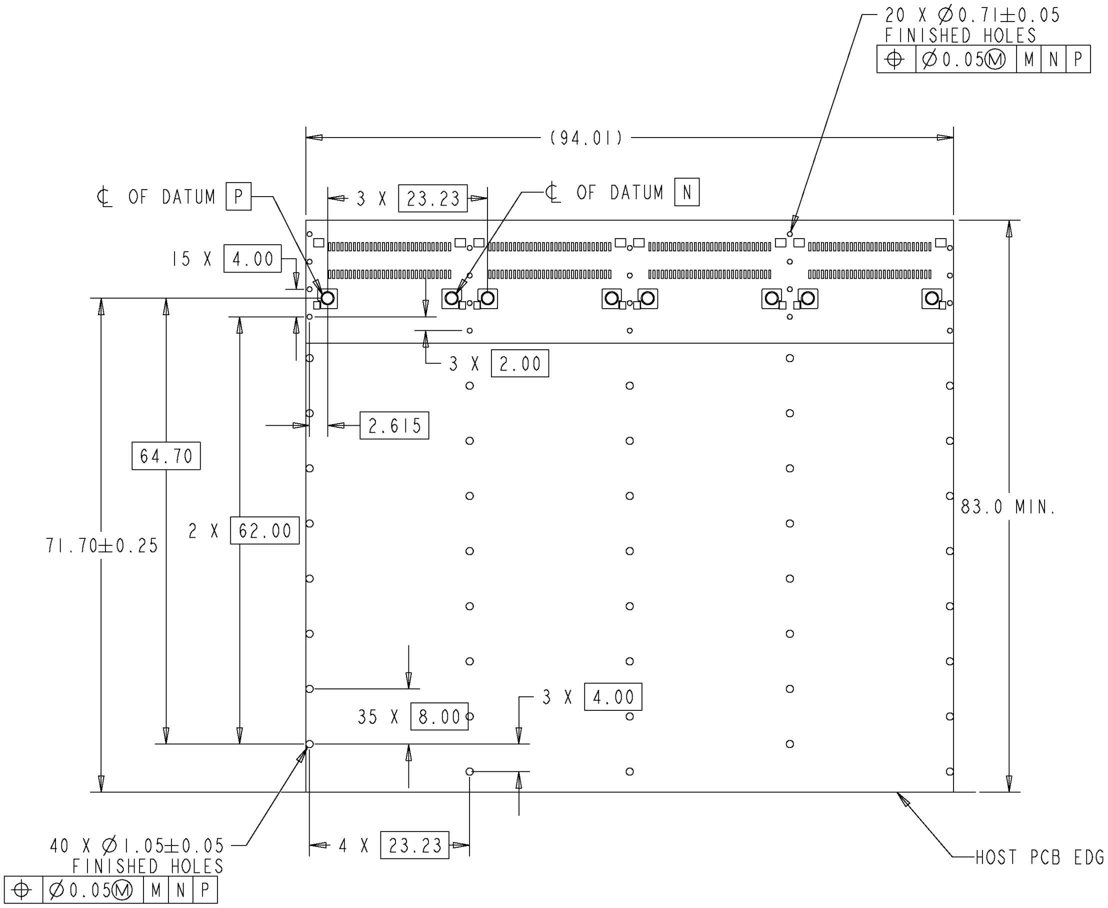


Figure 5-18: Host PCB layout for 1x4 cage

Figure 5-19 compares the host PCB layout between the 1x1, 1x2 and 1x4. The details of the 1x2 PCB layout are not given in this document.

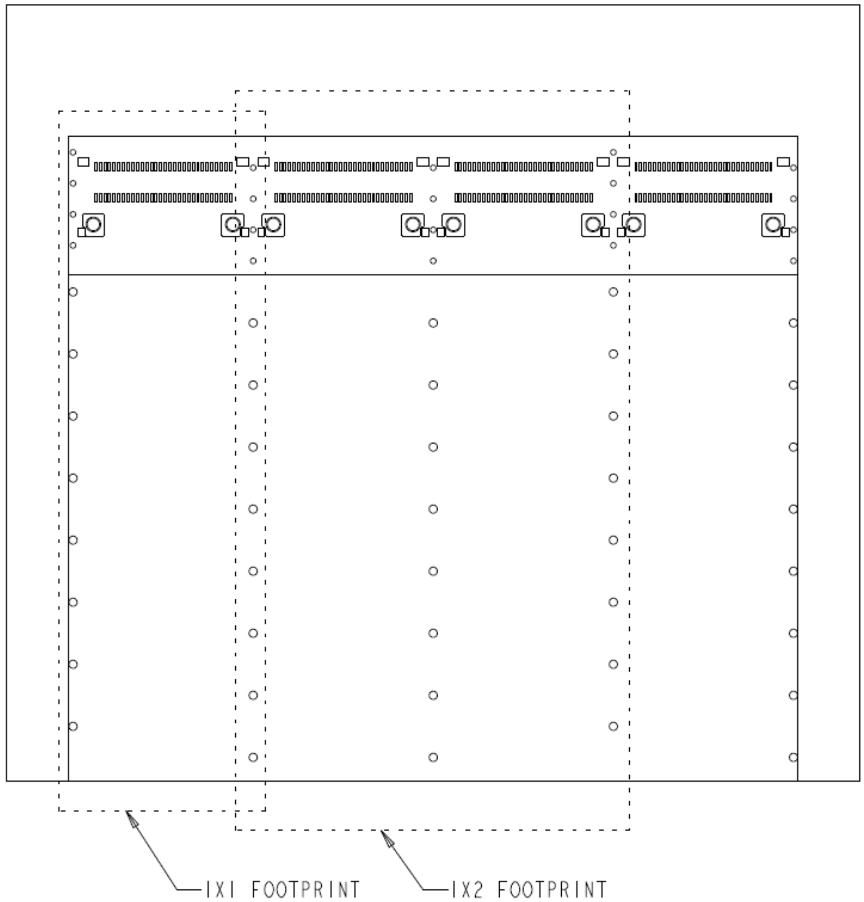


Figure 5-19: Comparison of host PCB layout between 1x1, 1x2 and 1x4

5.8 Latch Flaps in Cage

In the cage, the flaps shown in Figure 5-20 and Figure 5-21 shall be on both sides of the cage to latch the module into the cage. Flaps are shown in a 1x1 cage but can be applied to a ganged cage such as a 1x4 cage or any 1xN cage.

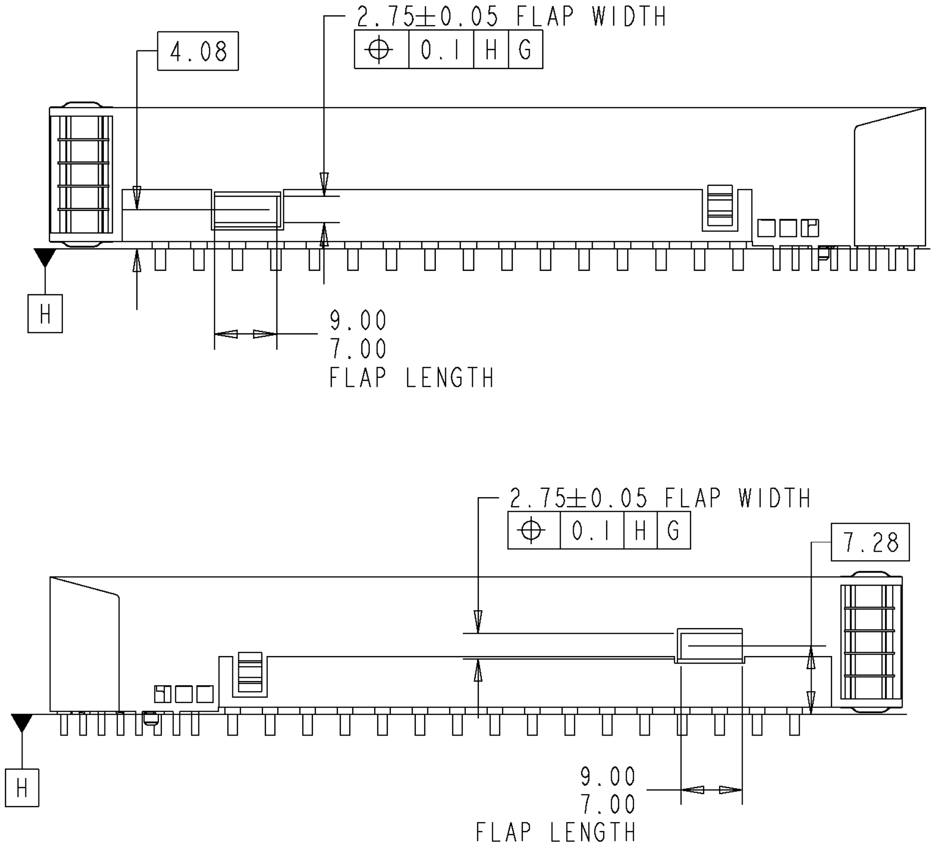


Figure 5-20: Latch feature, left and right side

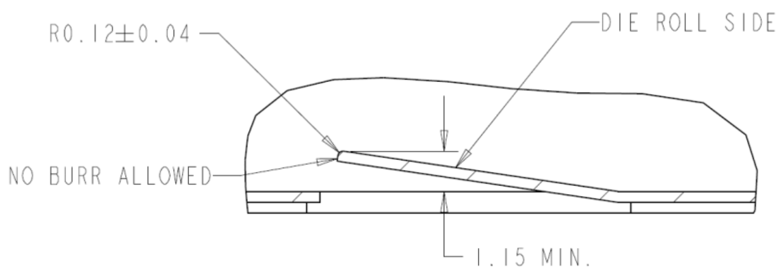


Figure 5-21: Latch flap, cross-sectional view from top, unmated condition

The cage latch flap shall be designed to meet the cage latch flap to module stop dimension of 44.80mm in mated condition, as shown in the Figure 5-22. Figure 5-22 is shown with a physical gauge, to compress the latch flap to the mated condition. See Appendix E for the detail of such gage. If the cage is to be inspected in its unmated condition, the cage height in the unmated condition should be considered so that the flap location meets the requirement in the mated condition. Cage latch flap can be inspected either with physical gauge to create the mated condition, or inspected under unmated condition and calculate the location under the mated condition.

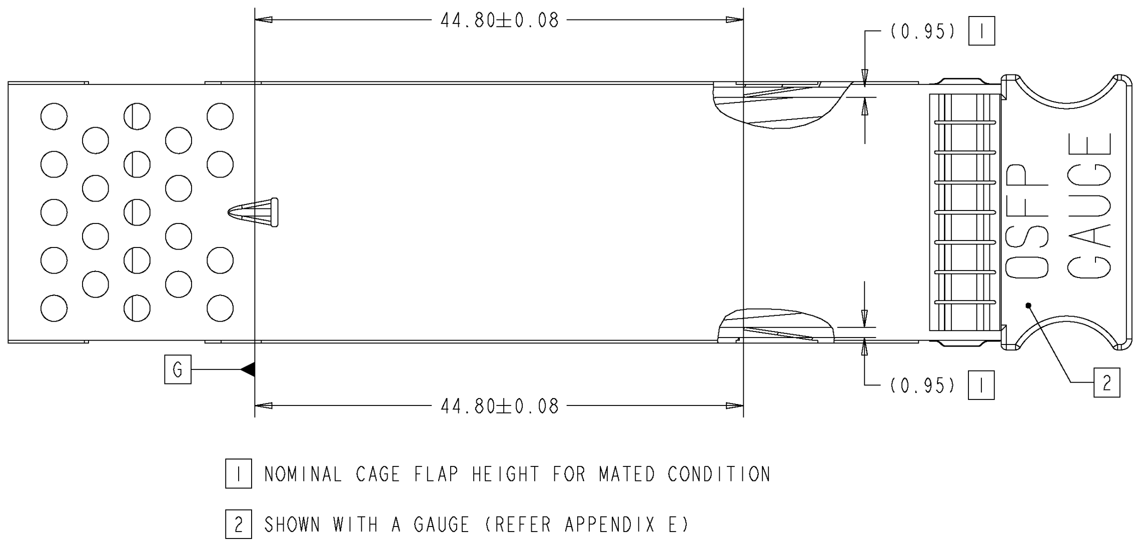


Figure 5-22: Latch flap, dimension from the positive stop

5.9 Bezel Panel Cut-Out

The EMI spring fingers of the cage shall make contact to the inside of the bezel panel cut out to make ground contact. Figure 5-23 and Figure 5-24 show the recommended dimensions of the bezel panel cut-out. With the horizontal pitch of the cage being 23.23mm, the bezel cut out width of 1x2 shall be 47.51mm while the detailed design is not depicted here.

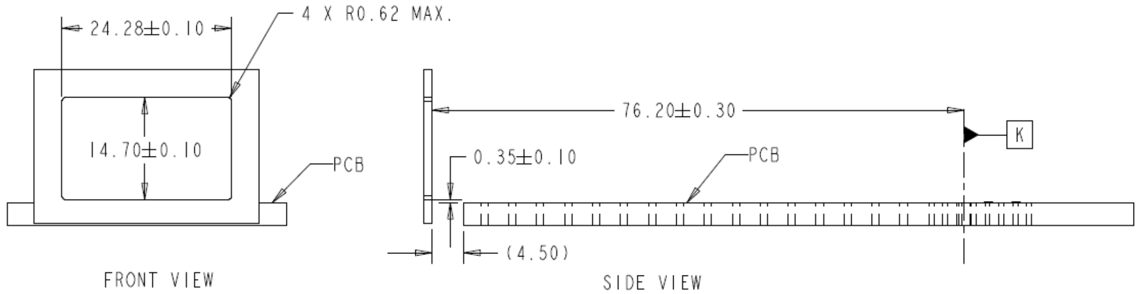


Figure 5-23: Bezel design and location for 1x1 cage

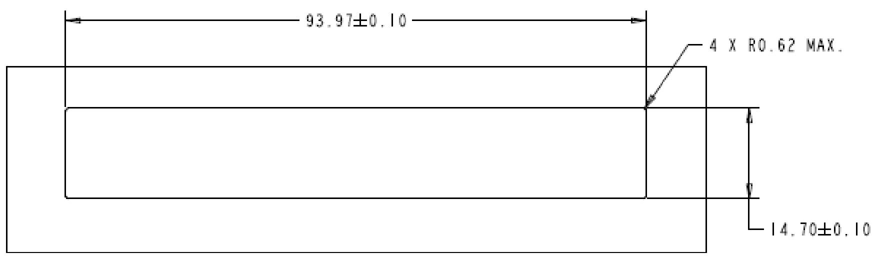


Figure 5-24: Bezel design for 1x4 cage

5.10 Single Row SMT Connector

The electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module and be expelled outside. The tail direction of the connector is specified as shown.

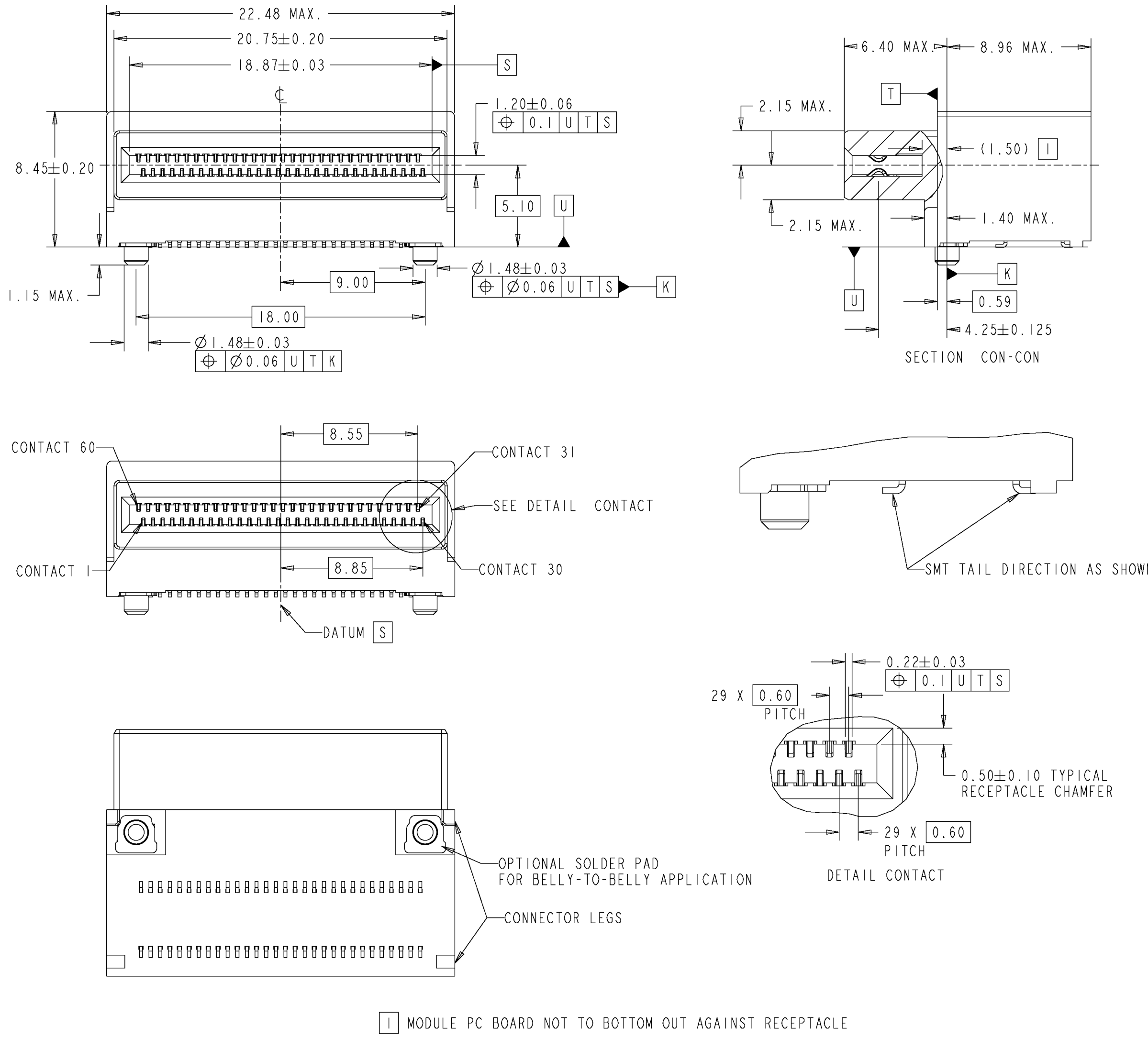


Figure 5-25: Surface mount connector

5.11 Blank Plug

Any unused or empty port of a cage shall have a blank plug. The blank plug shall serve to minimize EMI while at the same time allowing for a maximum airflow no more than that of a module. See Figure 5-26 for a recommended design. The blank plug shall be used on the stacked SMT (section 7) and stacked press-fit cage (section 8).

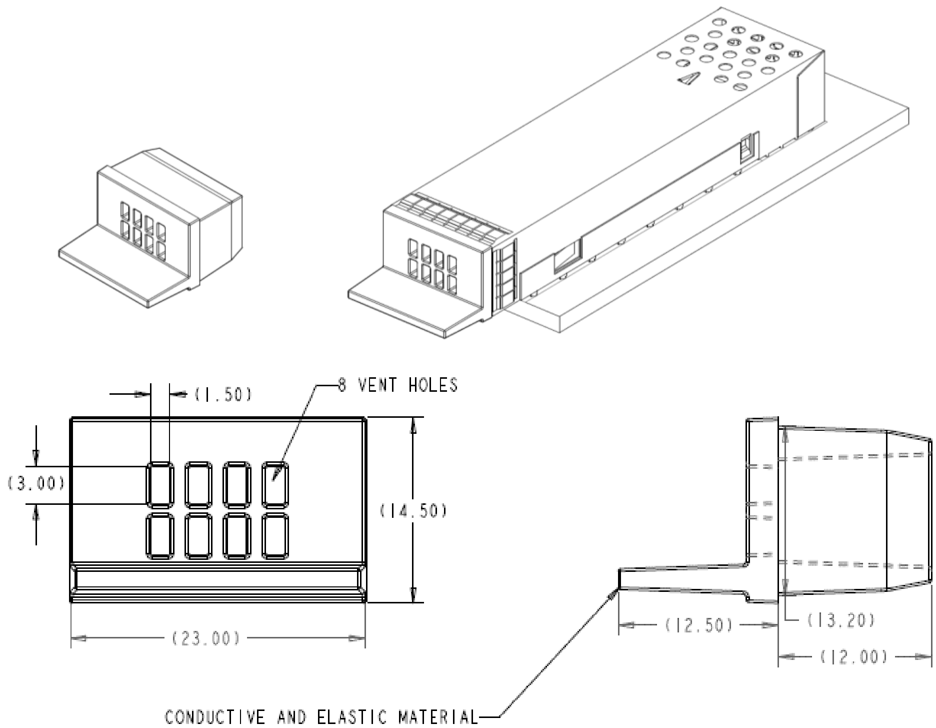


Figure 5-26: OSFP blank plug (reference design)

6 OSFP1600 Single Row Surface Mount Technology Connector and Its Cage: Mechanical Specification

This section describes the amended mechanical specification to section 5, which applies to the OSFP1600 cage and connectors. OSFP or OSFP800 may use the specification in this section.

The specifications of OSFP1600 shall be interpreted as applicable to SMT stacked, press-fit, or cabled connector/cages if they are used for OSFP1600.

6.1 Host PCB layout – 1x1 OSFP1600

For OSFP1600, this section will replace section 5.6.

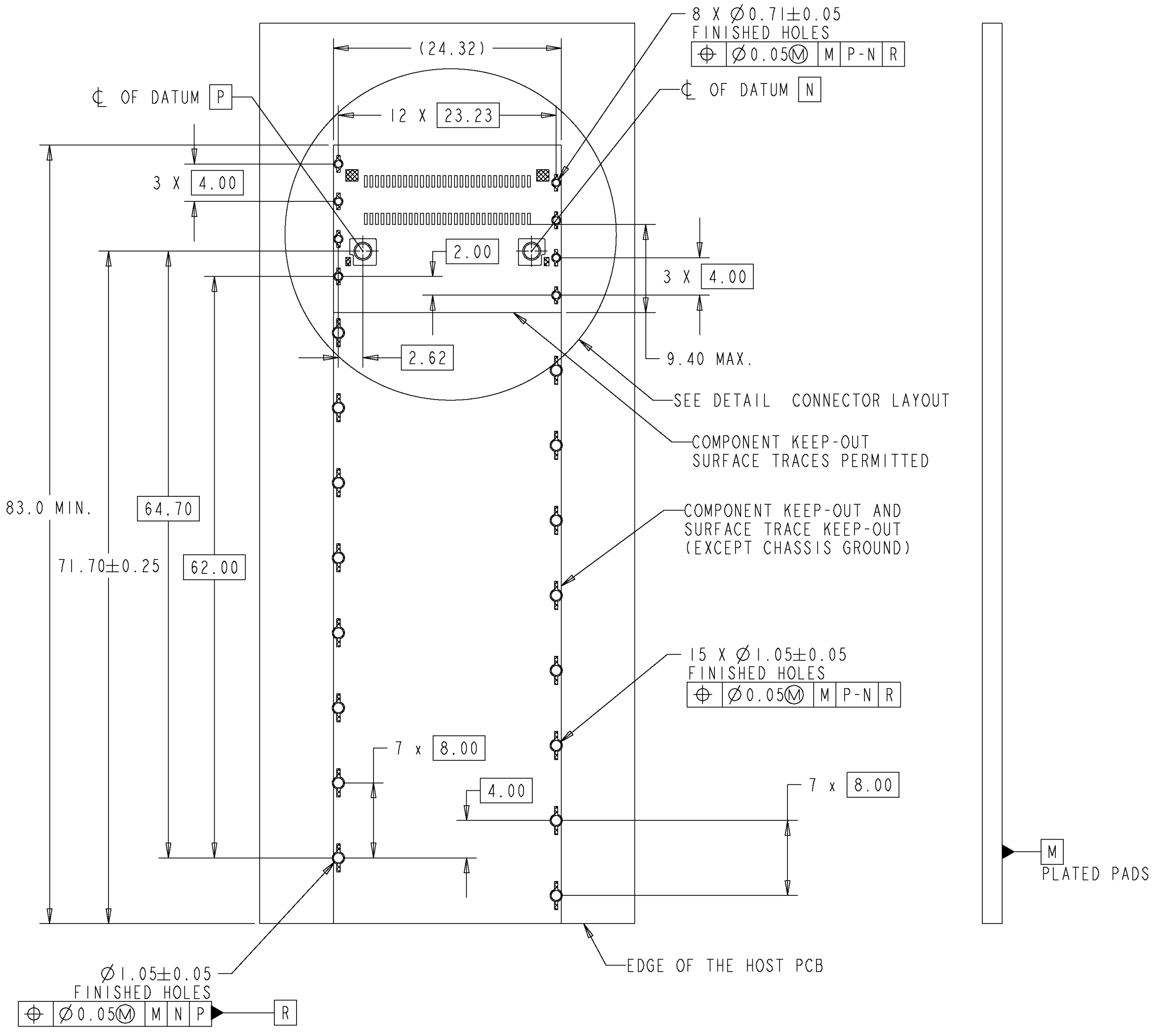


Figure 6-1: Host PCB layout for OSFP1600 1x1

Figure 6-1 shows the host footprint for OSFP1600. The connector seating plane, Datum M, is defined by the plated pads. Figure 6-2 shows the details of the footprint near the SMT connector. Figure 6-3 shows the details of the footprint where the cage pin is inserted. Figure 6-4 shows the details of the solder pads for the optional retention ring and the connector standoff.

Compared to OSFP and OSFP800, cage and the connector of OSFP1600 are seated on the plated pad, without solder. The areas where the connector standoffs touch down are reduced to ensure sufficient gap from the other plated pads. For the soldered area, solder paste thickness of nominal 0.127mm to be used.

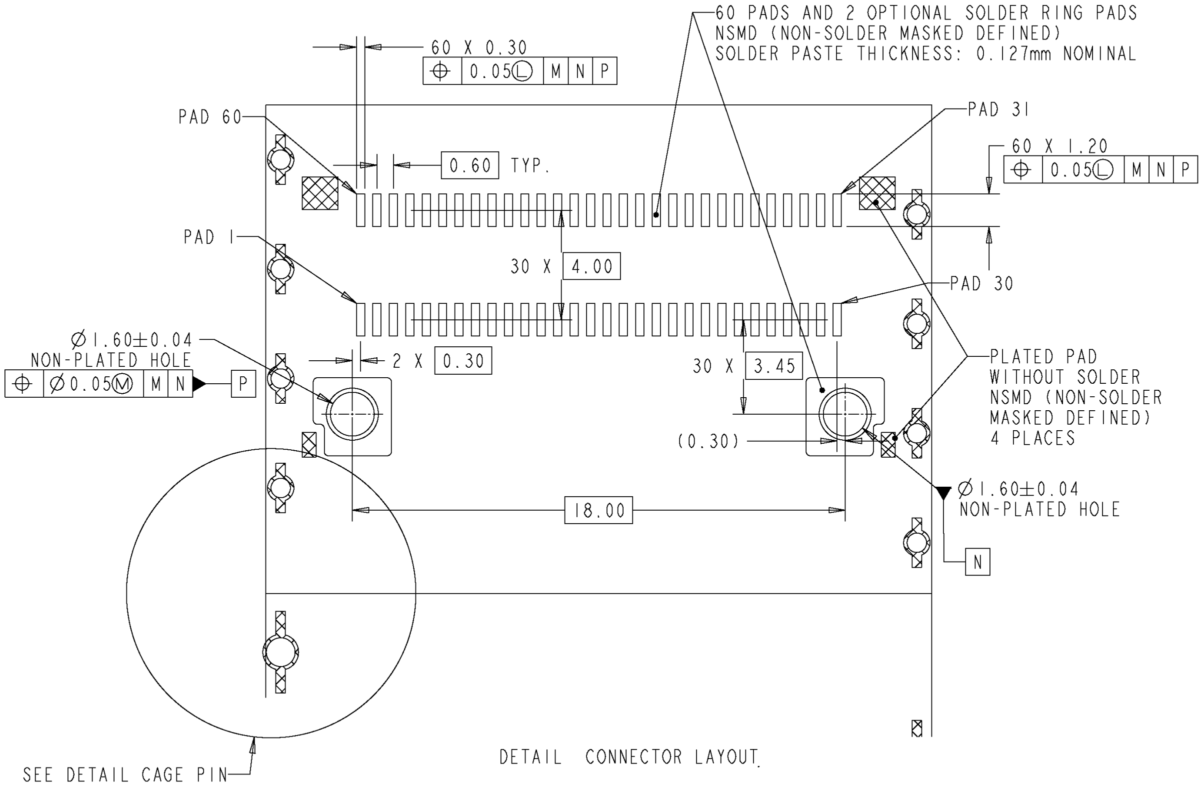


Figure 6-2: Host PCB layout for OSFP1600 (Detail Connector Layout)

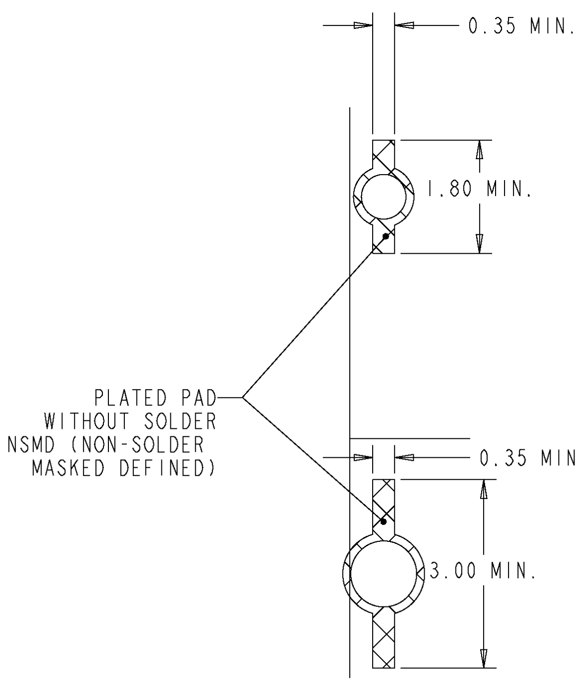


Figure 6-3: Plated pad for cage pin (Detail cage pin)

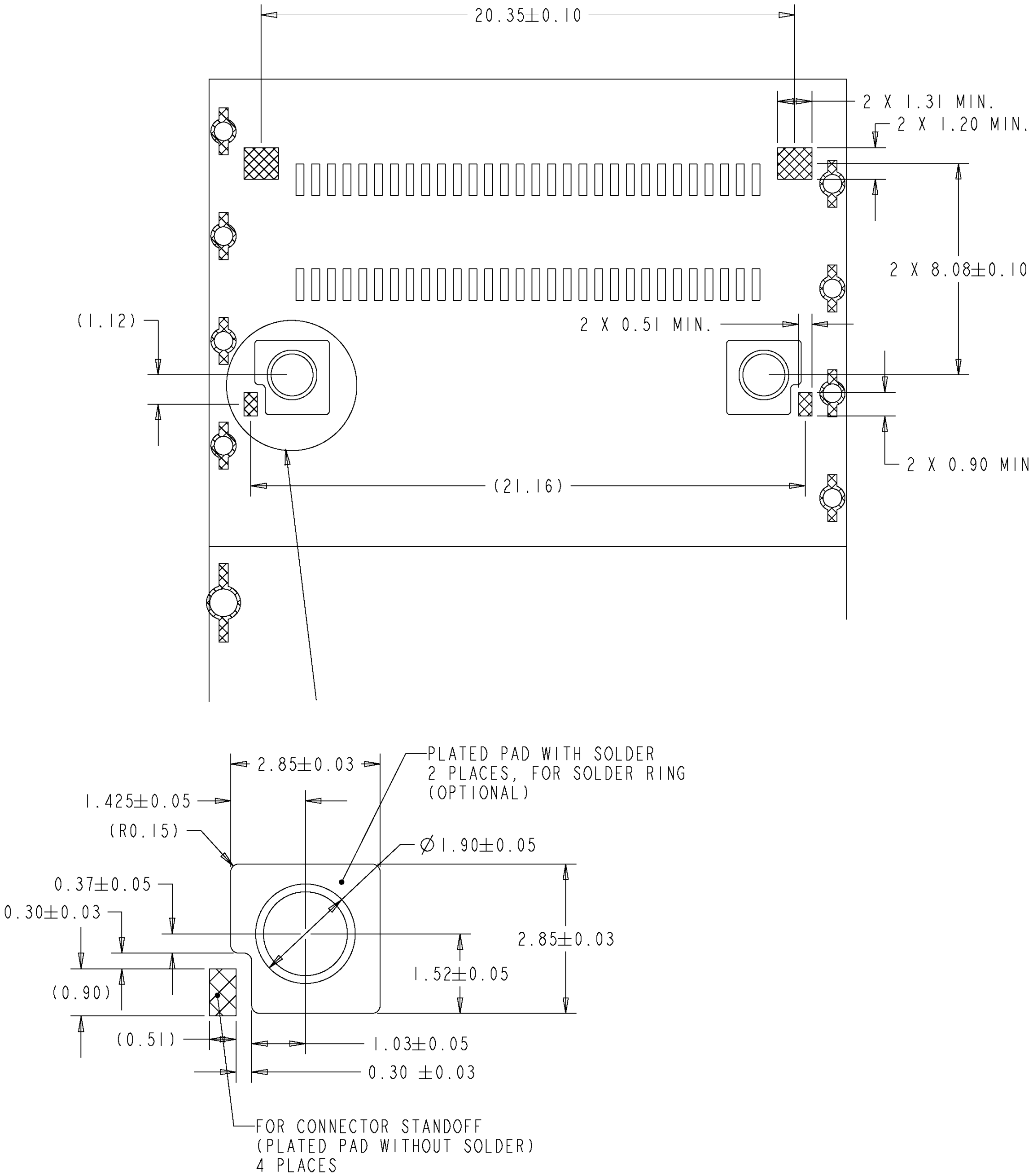


Figure 6-4: Connector standoff and pad for solder ring footprint, for OSFP1600

6.2 Latch Flap in Cage for OSFP1600

For OSFP1600, Figure 6-5 replaces Figure 5-22 of the latch flap location with respect to the module stop. OSFP1600 requires tighter tolerance in the latch flap location compared to OSFP and OSFP800.

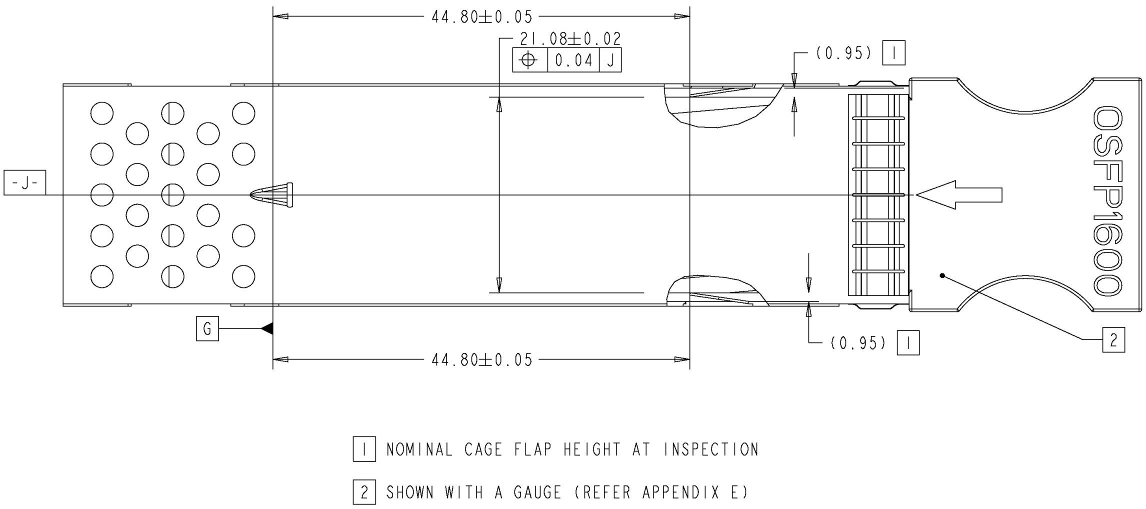


Figure 6-5: OSFP1600, cage latch flap, dimension from stop

6.3 OSFP1600 Single Row SMT Connector

Figure 6-6 amends Figure 5-25. All specifications in Figure 5-25 apply, except the dimension and notes shown in Figure 6-6. The connector seating plane (datum U) is defined by the standoffs. The contact points of the connector, in the mated condition, have tighter tolerance than what is allowed for OSFP and OSFP800.

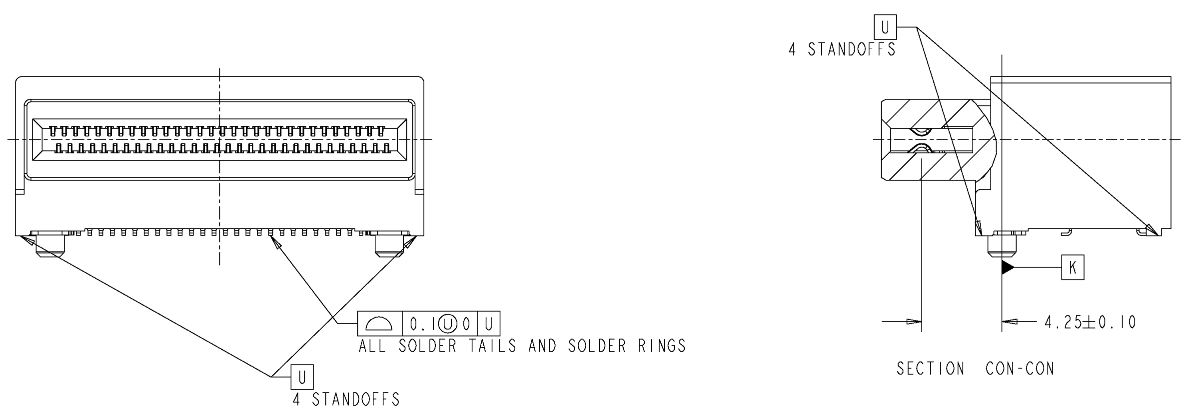


Figure 6-6: OSFP1600 SMT connector, datum and contact location

7 Stacked Surface Mount Technology Connector and Its Cage

7.1 Overview

In this section, the configurations of the stacked SMT connector and cage are presented. In one configuration depicted in section 7.2, the vertical pitch between the port is 14.9mm. This configuration can fit the OSFP modules densely. In another configuration depicted in section 7.3, the vertical pitch between the port is 19.9mm. In this configuration, a riding heatsink can be placed to the OSFP modules for improved thermal capabilities.

Figure 7-1 gives an overview of a 2x1 SMT connector, cage, host PCB and the panel of 14.9mm pitch configuration and 19.9mm pitch configuration. Figure 7-2 is front view of the cage only, which shows the difference in the vertical pitch between the ports.

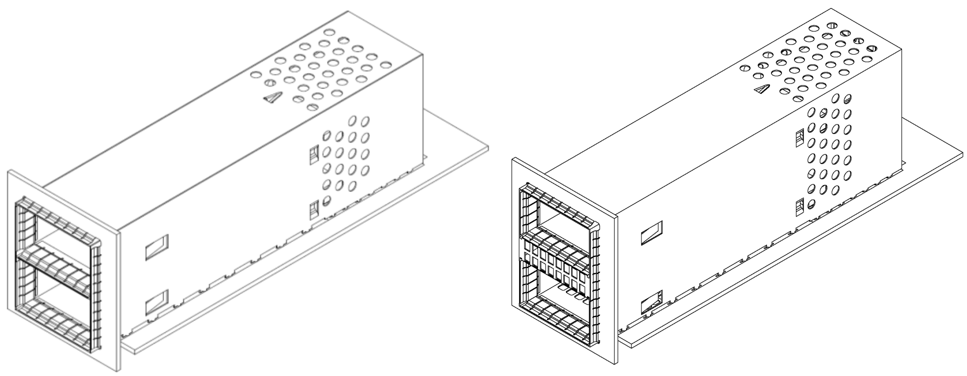


Figure 7-1: Stacked SMT 2x1 cage, 14.9mm pitch (left) and 19.9mm pitch (right)

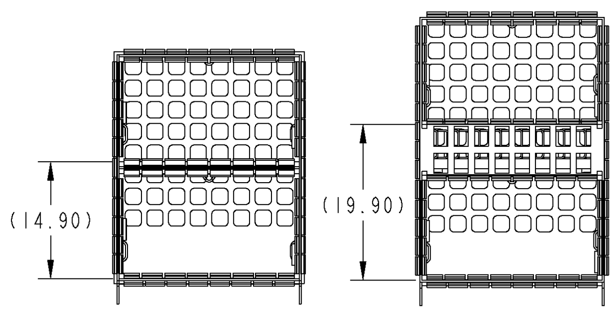


Figure 7-2: Front view of the Stacked SMT cage, 14.9mm pitch and 19.9mm pitch

Both configurations use same host PCB footprint as in the section 7.4. Table 7-1 shows the difference between the two configurations.

Table 7-1: Difference between the 14.9mm and 19.9mm pitch stacked

	Stacked cage and connector, 14.9mm pitch	Stacked cage and connector, 19.9mm pitch
Vertical Pitch	14.9mm	19.9mm
Riding Heatsink	No space for top side of bottom port	Able to place a riding heatsink on the top side of bottom port.
Supported module type	OSFP module type 1 and 2 (refer Figure 3.3); Type 3 cannot be plugged to the bottom port	OSFP module type 1,2 and 3
Application	OSFP400 and OSFP800; Tighter mechanical tolerance as specified in the notes of Figure 7-13 and Figure 7-16 should be implemented and connector should support OSFP1600, to support OSFP1600.	OSFP1600, assuming the connector support OSFP1600. Same connector/cage can be used for OSP400 and OSFP800 also (See Table 4).

7.2 Stacked SMT Cage and connector, 14.9mm Pitch

7.2.1 Overview

Left figure of Figure 7-1 gives an overview of a 2x1 SMT connector, cage with 14.9mm vertical pitch.

In the mechanical drawings of this section, the datum as defined in Table 7-2 shall apply. Note that the same designators are used for the corresponding features of the single row SMT connector and its cage, as in Table 5-1.

Table 7-2: Descriptions of the Stacked SMT cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 7-3
H	Seating plane of Cage on host pc board	Figure 7-3
J	Width of inside of Cage	Figure 7-4
K	Connector guide post #1	Figure 7-15
L	Cage Pin #1	Figure 7-3
M	Top surface of host pc board.	Figure 7-30
N	Host pc board through hole #1 to accept Connector guide post	Figure 7-30
P	Host pc board through hole #2 to accept Connector guide post	Figure 7-30
R	Host pc board through hole #1 to accept Cage Pin	Figure 7-30
U	Seating plane of Connector	Figure 7-15

For features of latch, stop and keying which are not specified in the mechanical drawings in this section, the same specification as the single row SMT connector and its cage in section 5 or section 6 shall apply.

7.2.2 Cage Dimensions and Positioning Pin

Figure 7-3 through Figure 7-5 show the cage datum, positioning pin, port size, and cage height of the cage with 14.9mm vertical pitch. Figure 7-6 shows that the middle row compliance pins in the 1x4 cage should be shorter than the others to support belly-to-belly applications.

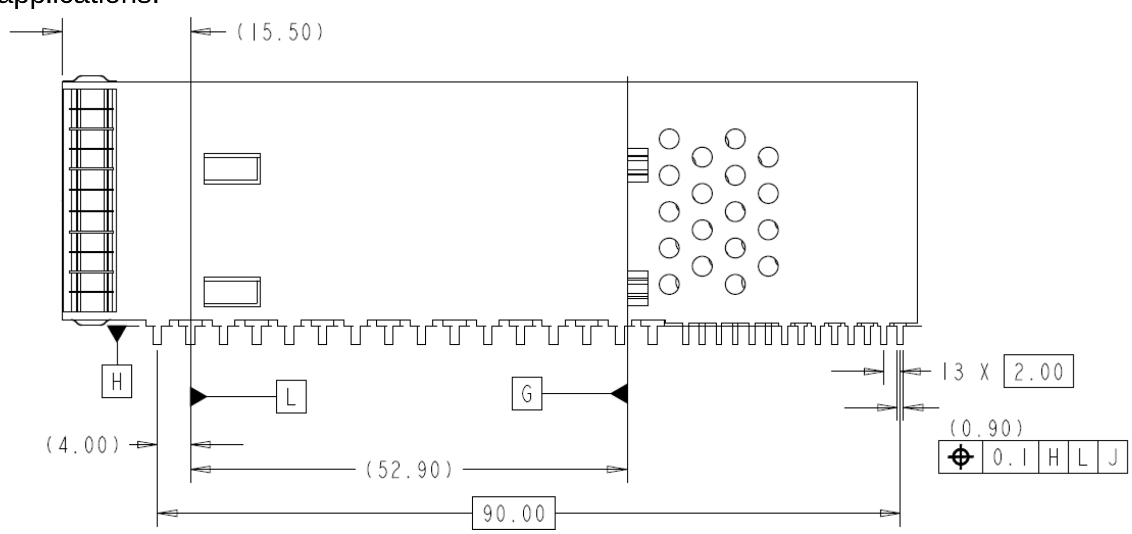


Figure 7-3: Cage positioning pins and forward stop

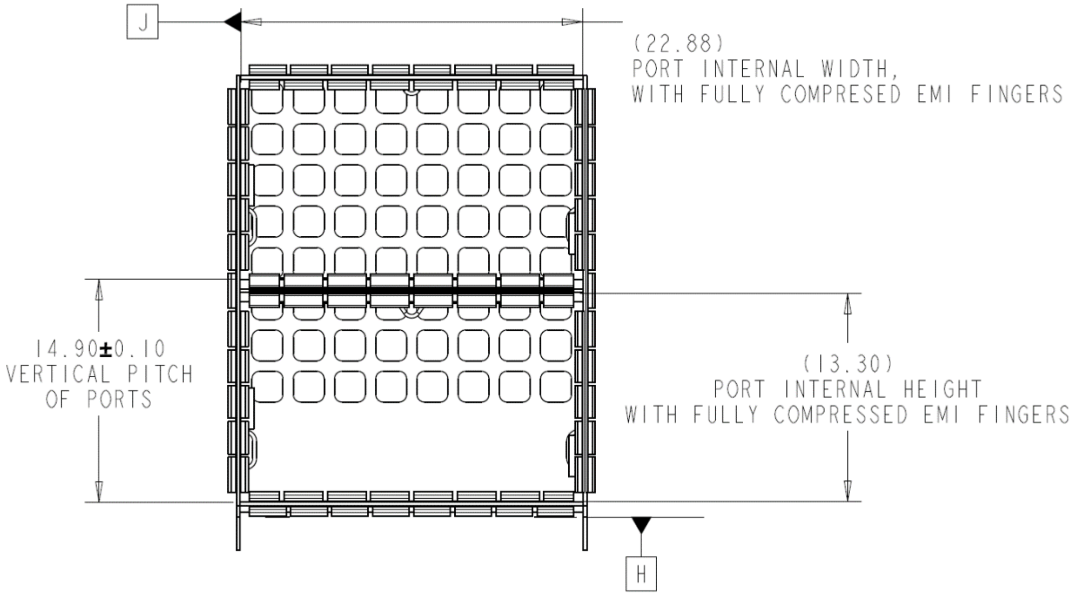


Figure 7-4: Port internal width, height and vertical pitch, 14.9mm pitch

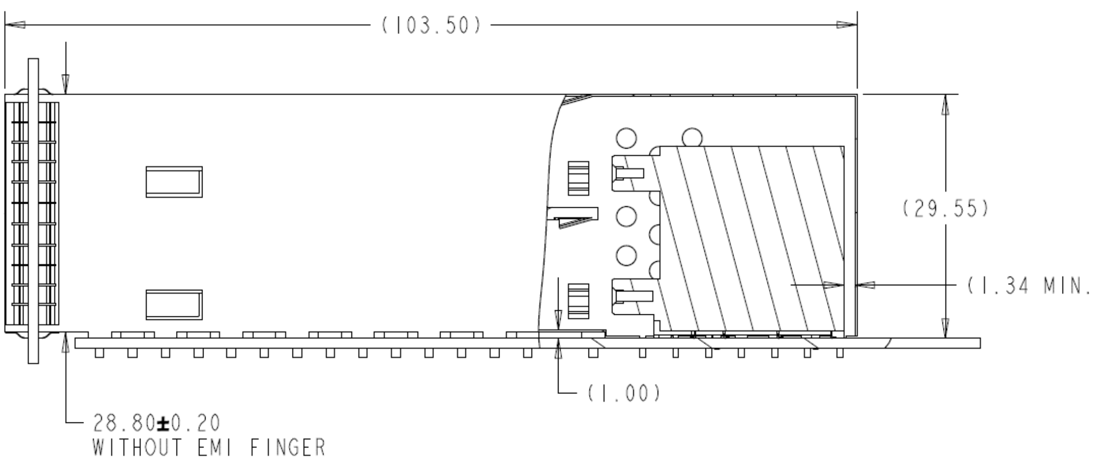


Figure 7-5: Side view of 2x1 cage with vertical cage dimensions, 14.9mm pitch

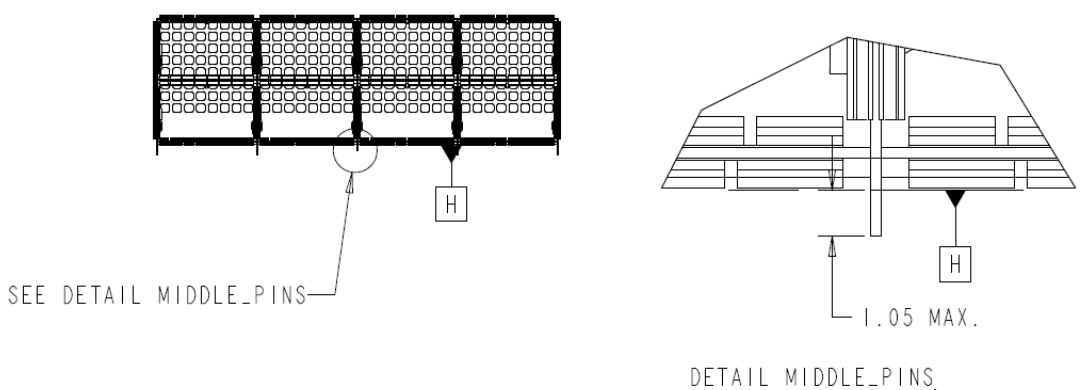


Figure 7-6: Length of the compliance pins at the middle, for belly-to-belly applications

7.2.3 Ventilation Holes

Cages should have ventilation holes to allow for sufficient airflow. Figure 7-7, Figure 7-8 and Figure 7-9 show an example design. Ventilation pattern may be different with example, but there should be ventilation on the top, side and the rear. Bottom ventilation as in the Figure 7-10 is optional.

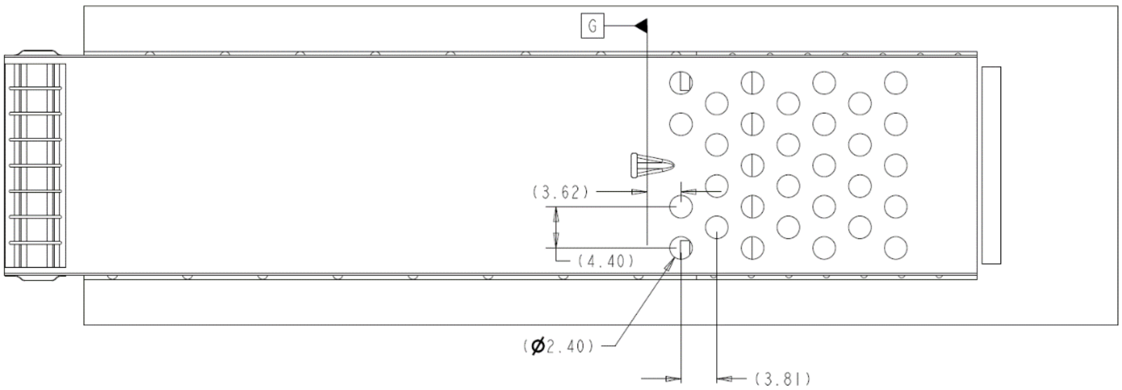


Figure 7-7: Top ventilation, example design

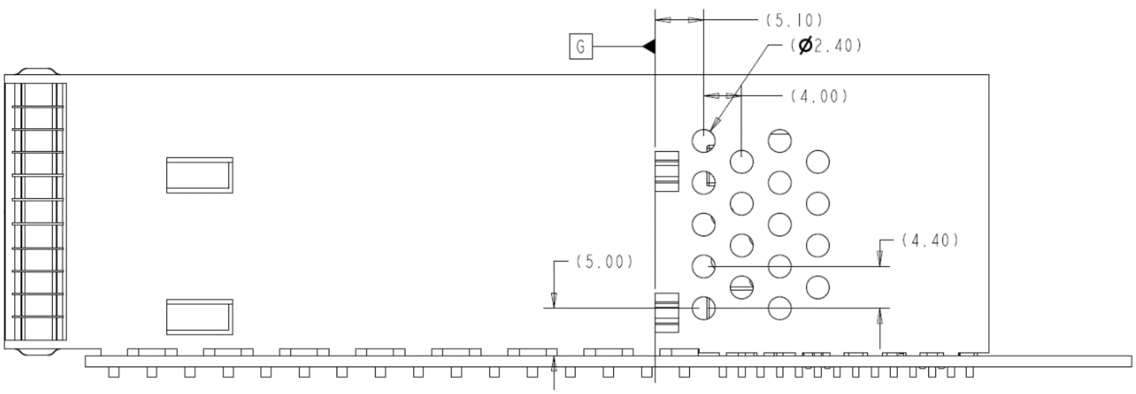


Figure 7-8: Side ventilation, example design

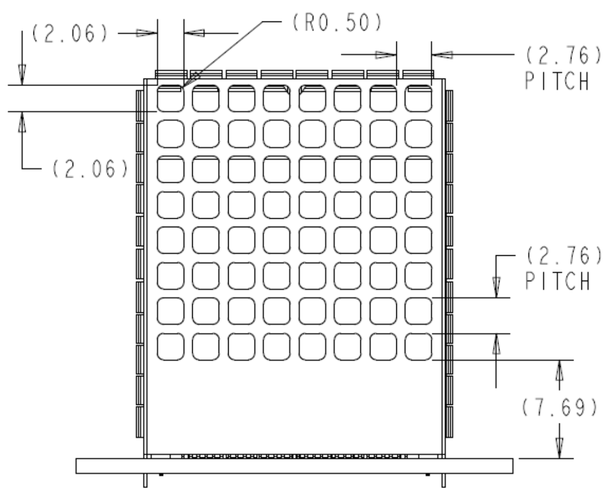


Figure 7-9: Rear ventilation, example design

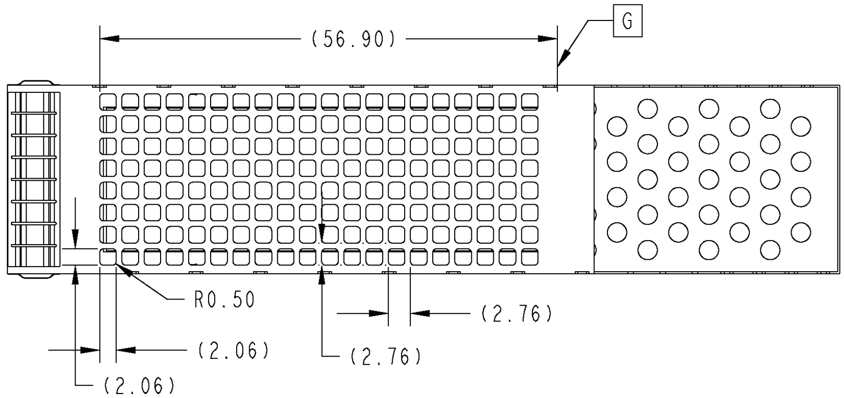


Figure 7-10: Bottom ventilation, example design

7.2.4 Bezel Panel Cut-Out

In this section, the recommended shape for the bezel to make contact with the EMI finger of the cage for 14.9mm vertical pitch is presented.

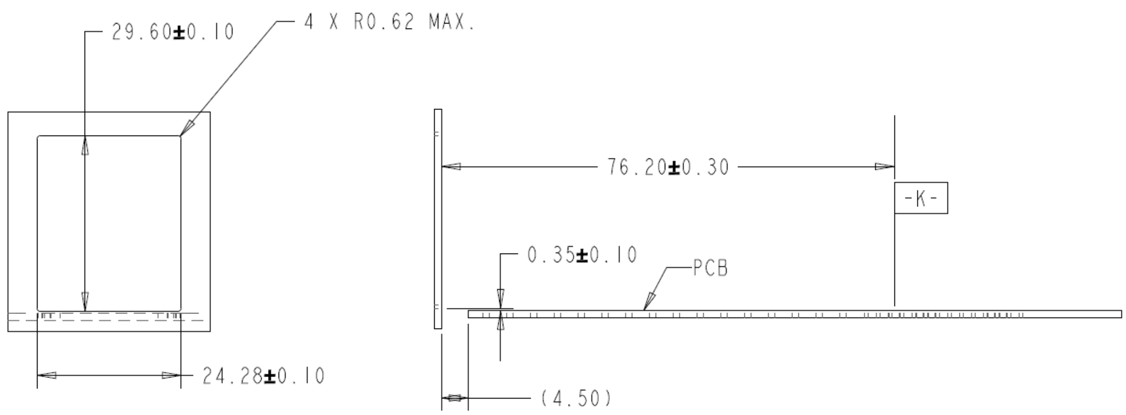


Figure 7-11: Bezel design and location for SMT 2x1 cage, 14.9mm pitch

7.2.5 Cage Latching Flap

The vertical location of the cage latching flap is shown in the Figure 7-12, which complies with single row cage in Figure 5-20 except they are stacked. Figure 7-13 shows the location of the latching flap with respect to the forward stop; Note that the tolerance shown in the figure is for OSFP400 and OSFP800 application, and tolerance for OSFP1600 is specified in the notes below the Figure 7-13.

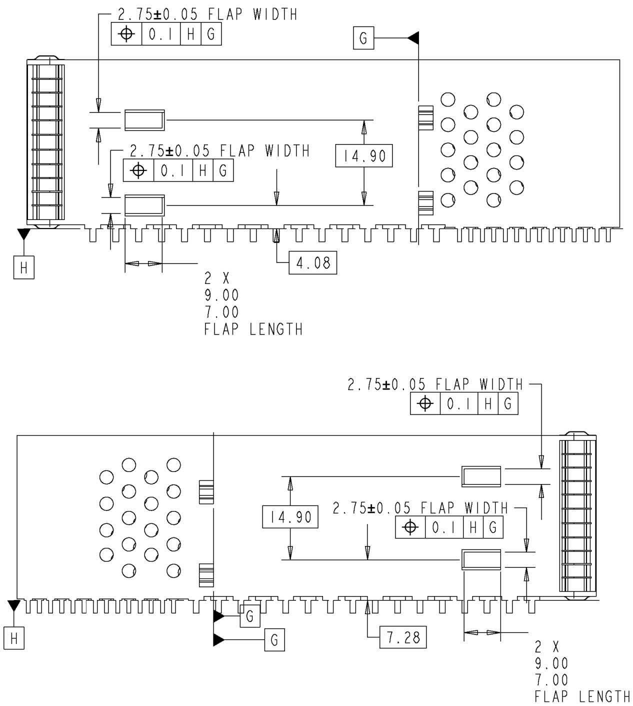
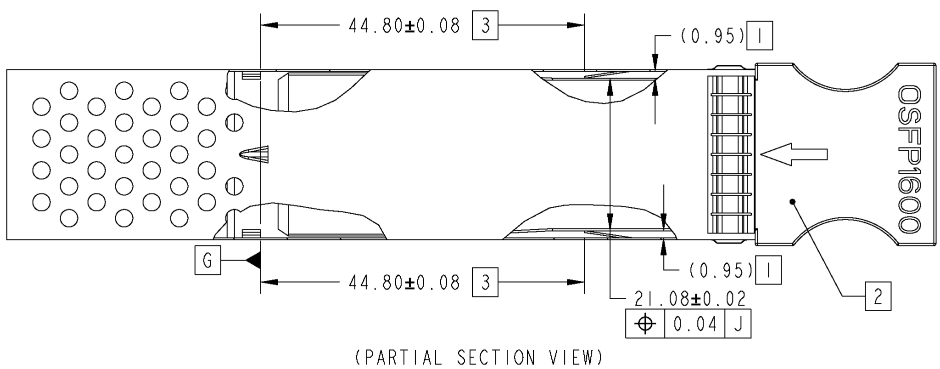


Figure 7-12: Latching flap size and location, 14.9mm pitch



1 NOMINAL CAGE FLAP HEIGHT AT INSPECTION

2 SHOWN WITH A GAUGE (REFER APPENDIX)

3 44.80±0.05 FOR CAGE TO USED WITH OSFP1600 APPLICATION

Figure 7-13: Latching flap location to forward stop, 14.9mm pitch

7.2.6 Stacked SMT Connector, 14.9mm Pitch

Figure 7-14 to Figure 7-17 show the maximum mechanical envelope of the stacked SMT connector for 14.9mm vertical pitch. The actual connector shape shall be smaller than this envelope. Figure 7-18 shows an example design, where the connector is optimized to provide better airflow to the bottom row. For the contact and peg dimensions, specifications as defined in section 4.9 or section 6.3 for the single row SMT connector shall be applied.

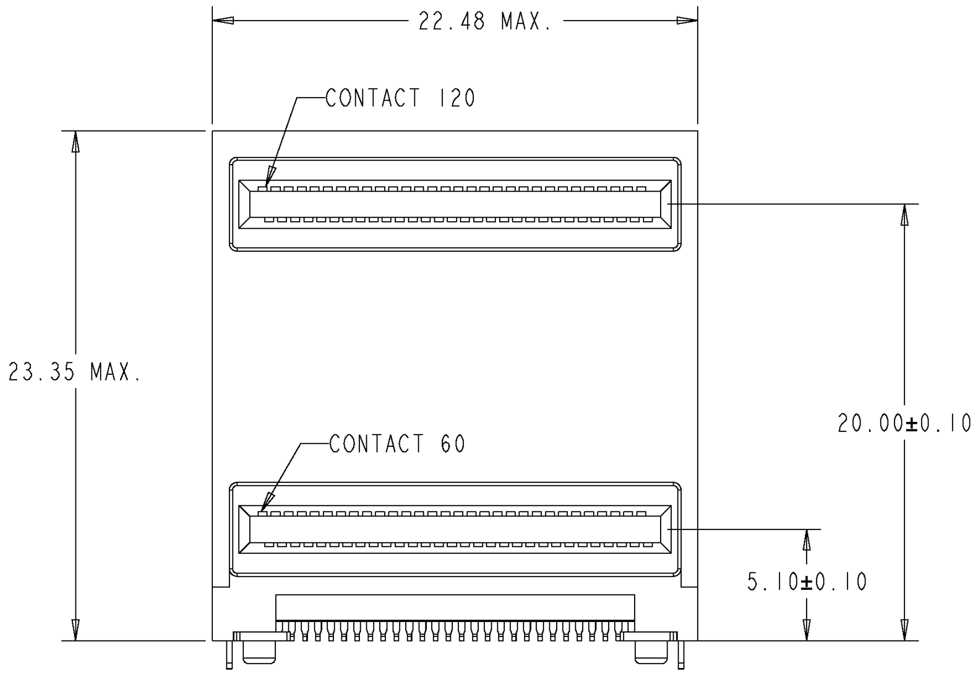


Figure 7-14: Stacked SMT connector, front view, 14.9mm pitch

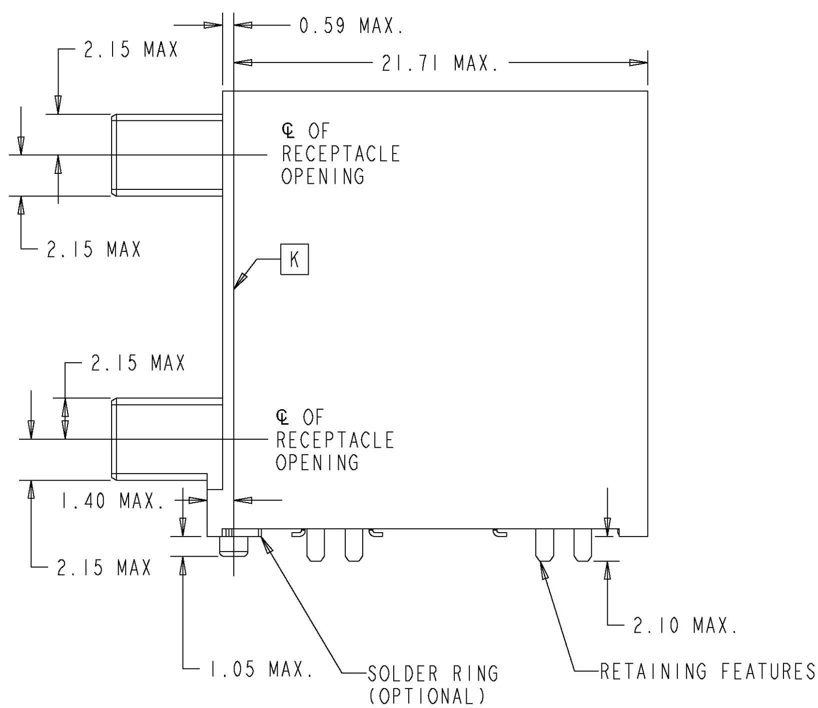


Figure 7-15: Stacked SMT connector, side view

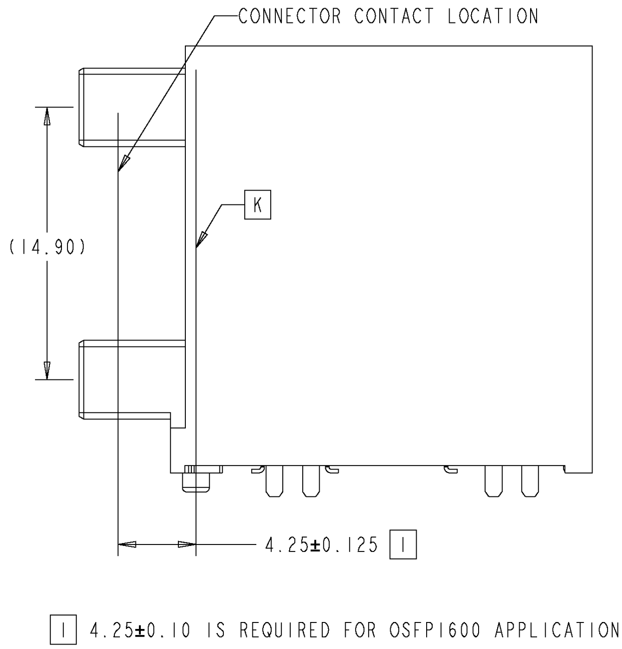


Figure 7-16: Stacked SMT connector, contact location, 14.9mm pitch

Figure 7-16 shows the location of the connector contact, where the connector make electrical connections with the module paddle card.

The retaining feature in Figure 7-15 should be designed to allow proper retention of the connector during and after soldering. The SMT tail direction shall be as defined in Figure 7-17.

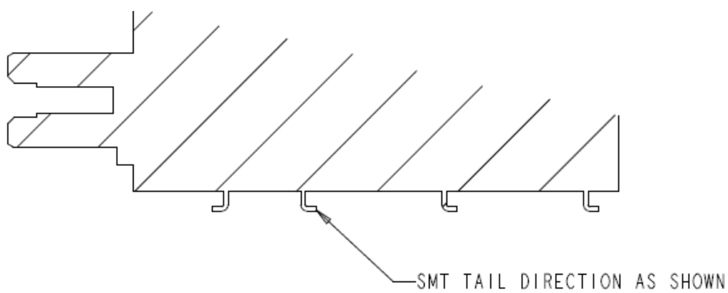


Figure 7-17: SMT tail direction

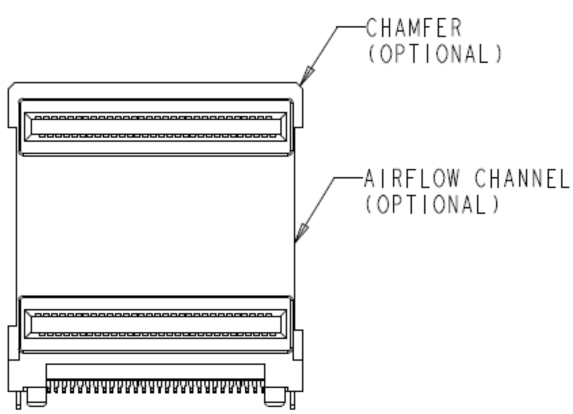


Figure 7-18: Example of actual connector design

7.3 Stacked SMT Cage and connector, 19.9mm Pitch

7.3.1 Overview

Right figure of Figure 7-1 gives an overview of a 2x1 SMT connector, cage with 19.9mm vertical pitch. It is taller by 5mm from the 14.9mm vertical pitch cage and connector. This 19.9m vertical pitch configuration have same host board footprint as in the section 7.4, and can have a riding heatsink for the bottom port.

In the mechanical drawings of this section, the datum as defined in Table 7-2 shall apply. For specification already defined in the section 7.2 for 14.9mm vertical pitch configuration shall be applied to this configuration as well, unless the specification is related with the vertical pitch of the cage and connector or defined in this section.

7.3.2 Cage Dimension and Positioning Pin

Figure 7-19 through Figure 7-21 show the cage datum, positioning pin, port size, and cage height of the cage with 19.9mm vertical pitch. It shows that this cage follows same specification with 14.9mm vertical pitch cage, except the vertical pitch and the height of the cage.

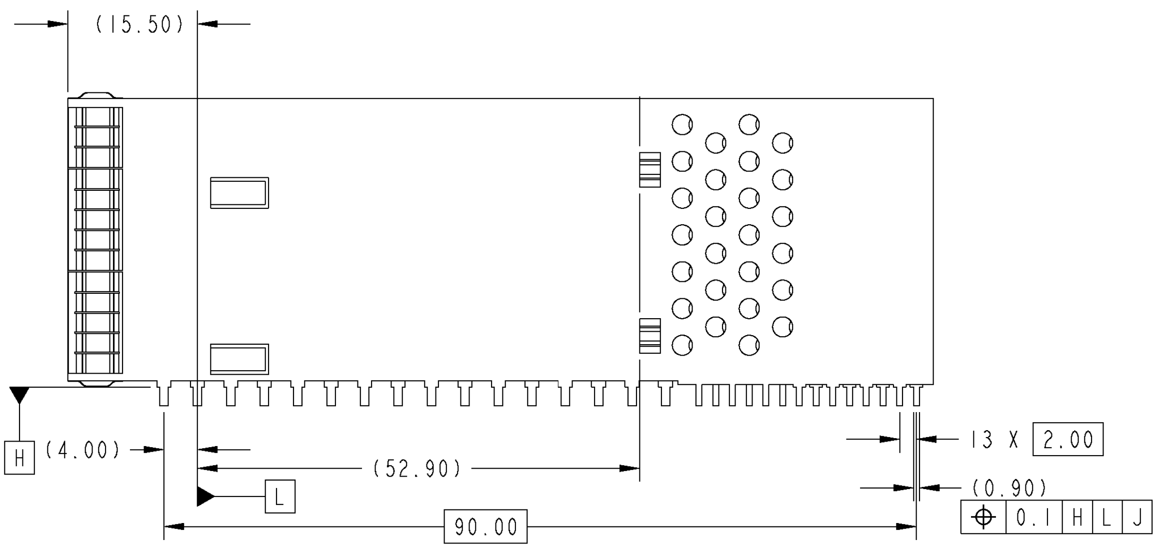


Figure 7-19: Cage positioning pins and forward stop

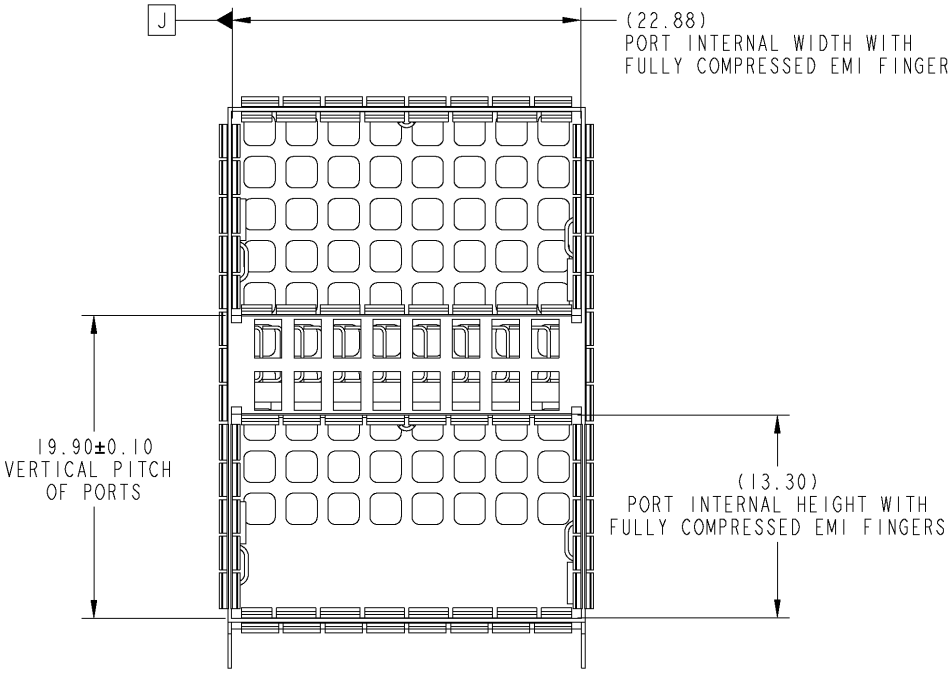


Figure 7-20: Port internal width, height and vertical pitch,19.9mm pitch

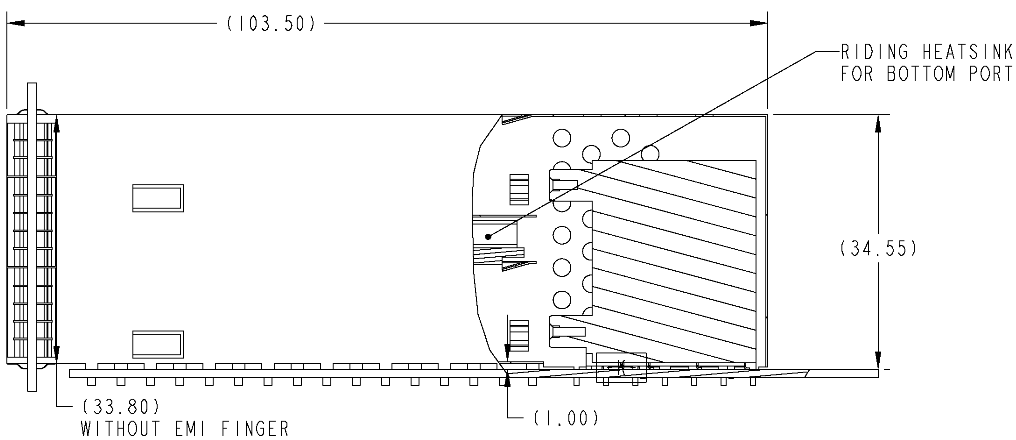


Figure 7-21: Side view of 2x1 cage with vertical cage dimensions, 19.9mm pitch

7.3.3 Ventilation Holes

Figure 7-22 and Figure 7-23 shows the side and rear ventilation example design.

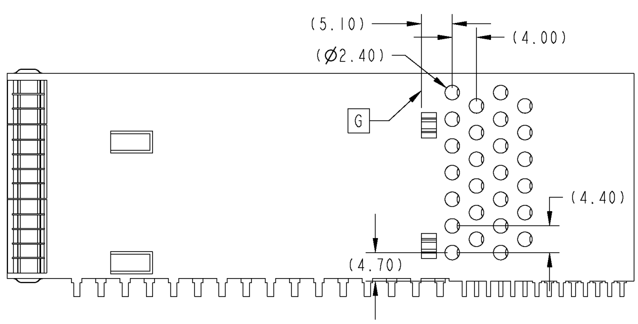


Figure 7-22: Side ventilation, example design, 19.9mm pitch

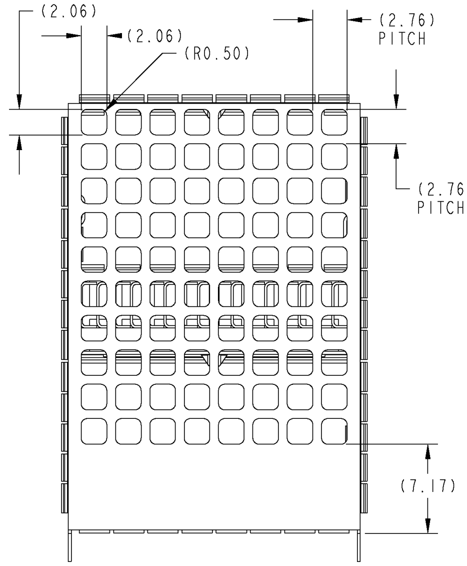


Figure 7-23: Rear ventilation, example design, 19.9mm pitch

7.3.4 Bezel Cut-Out

In this section, the recommended shape for the bezel to make contact with the EMI finger of the cage for 19.9mm vertical pitch is presented.

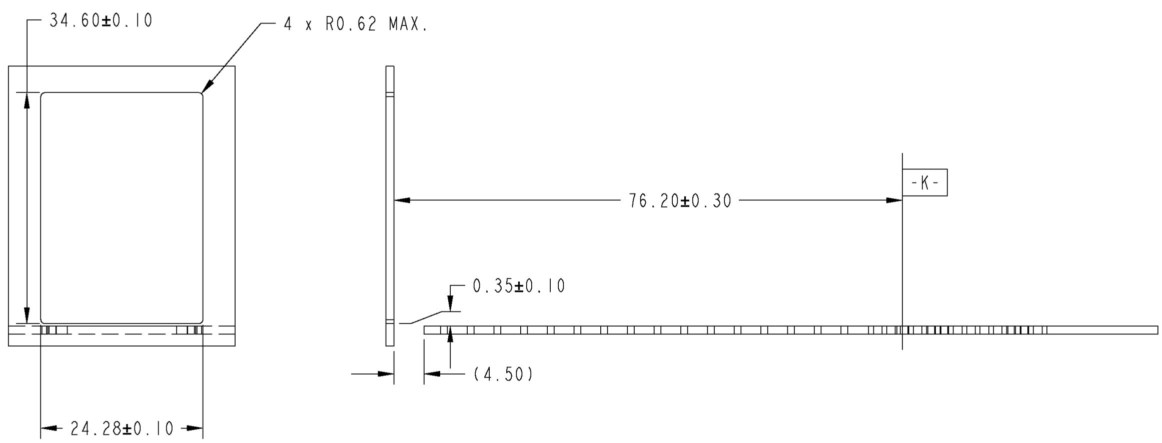


Figure 7-24: bezel design for SMT 2x1 cage, 19.9mm pitch

7.3.1 Cage Latching Flap

In Figure 7-25 and Figure 7-26, latching feature of the cage is shown. Note that when compared with the stacked cage of 14.9mm pitch, the default tolerance for the distance from the cage flap to the forward stop is tighter, so that the cage is compatible with OSFP1600 application.

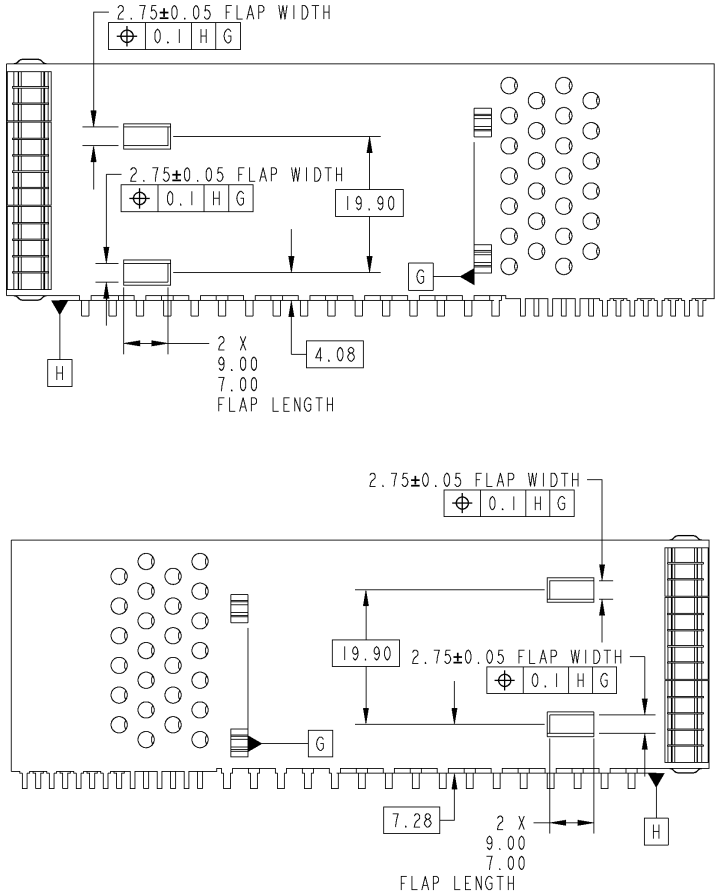


Figure 7-25: Latching flap size and location, 19.9mm pitch stacked

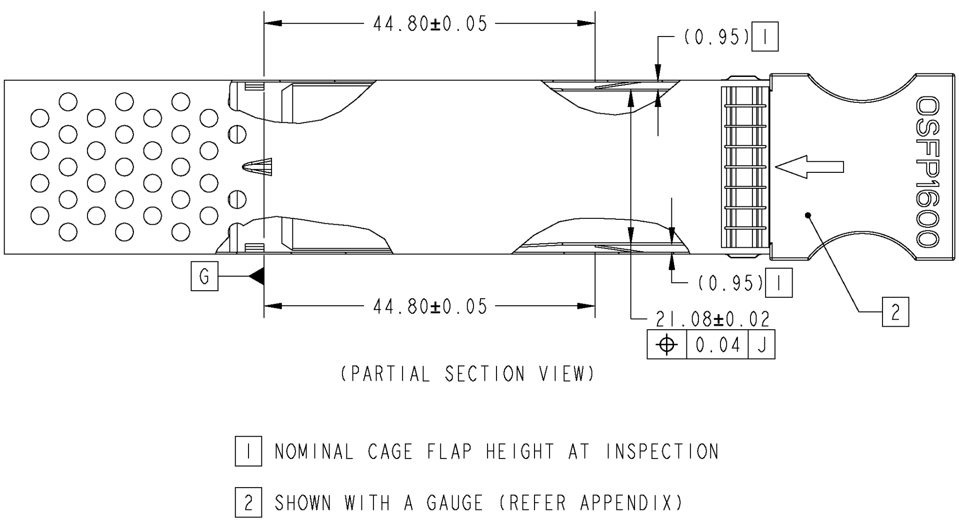


Figure 7-26: Latching flap location to forward stop, 19.9mm pitch stacked

7.3.2 Stacked SMT Connector

Figure 7-27 and Figure 7-28 show the maximum mechanical envelope of the stacked SMT connector for 19.9mm vertical pitch. The actual connector shape shall be smaller than this envelope. The connector has same dimensional requirement with the connector for 14.9mm vertical pitch as in the 7.2.6, except the pitch between the top and the bottom port.

For the contact and peg dimensions, specifications as defined in section 5.10 or section 6.3 for the single row SMT connector shall be applied.

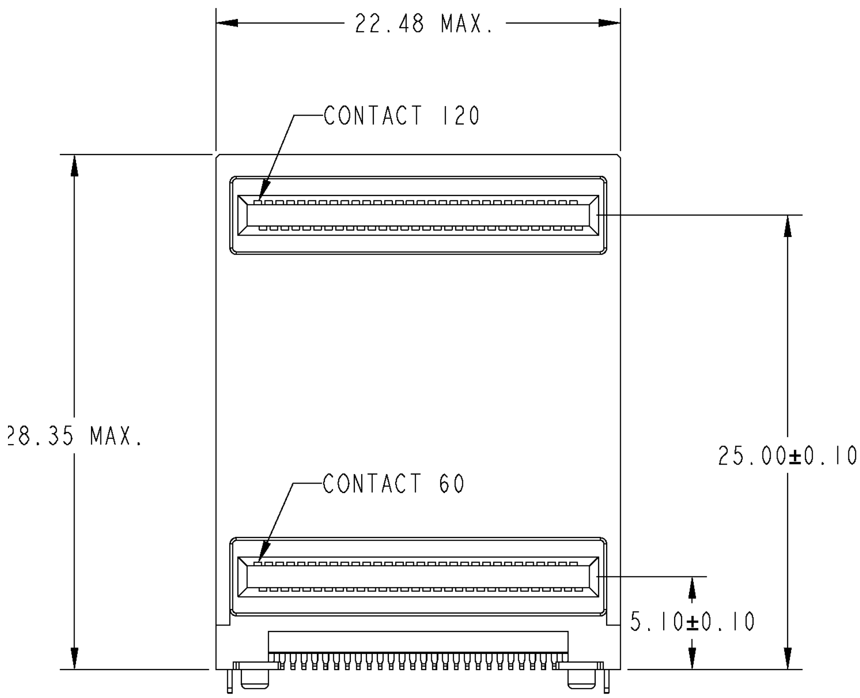


Figure 7-27: Stacked SMT connector, front view, 19.9mm pitch

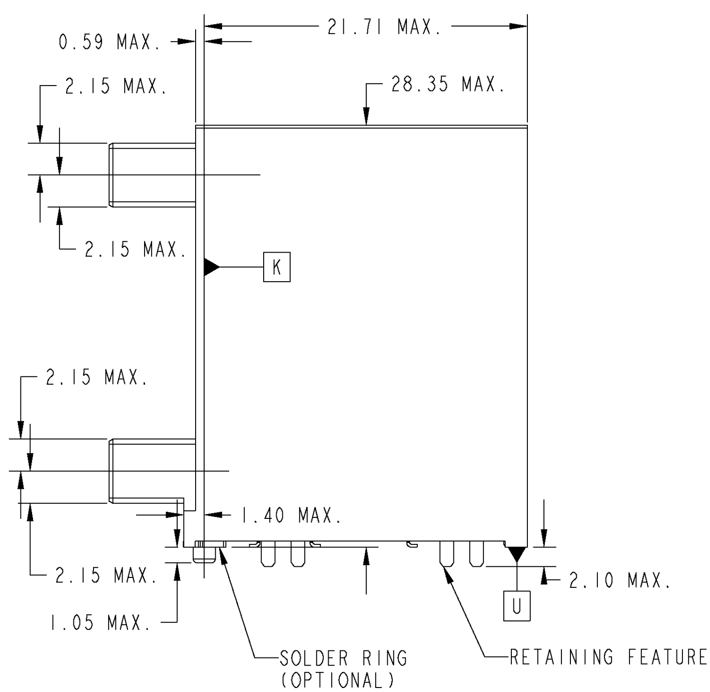


Figure 7-28: Stacked SMT connector, side view, 19.9mm pitch

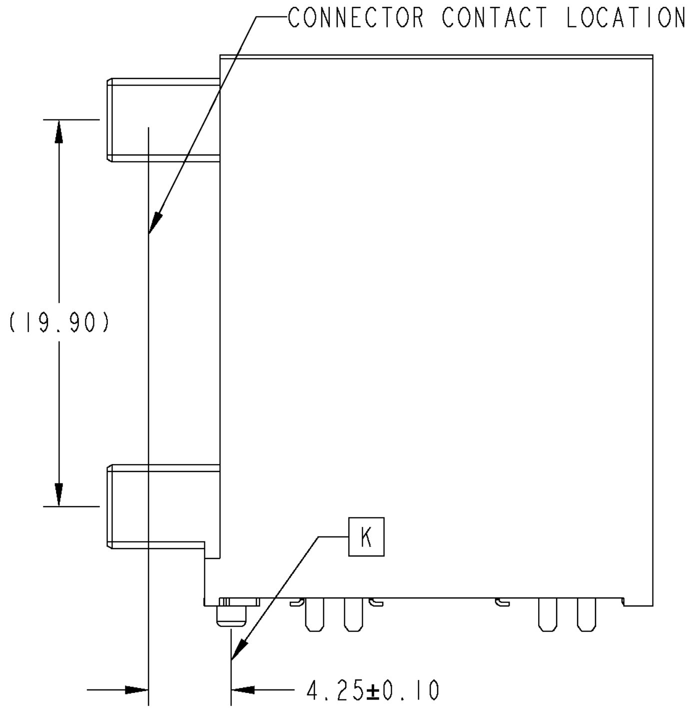


Figure 7-29: Stacked SMT connector, contact location, 19.9mm pitch

Figure 7-29 shows the location of the connector contact, where the connector make electrical connections with the module paddle card.

7.4 Host PCB Layout – 2x1 Cage

The host PCB layout pattern for 2x1 SMT connector and cage are presented in this section. Note that pads 1 to 60 correspond to pins 1 to 60 of the OSFP in the lower port as in Figure 14-1, while pads 61 to 120 correspond to pins 1 to 60 of the OSFP in the upper port.

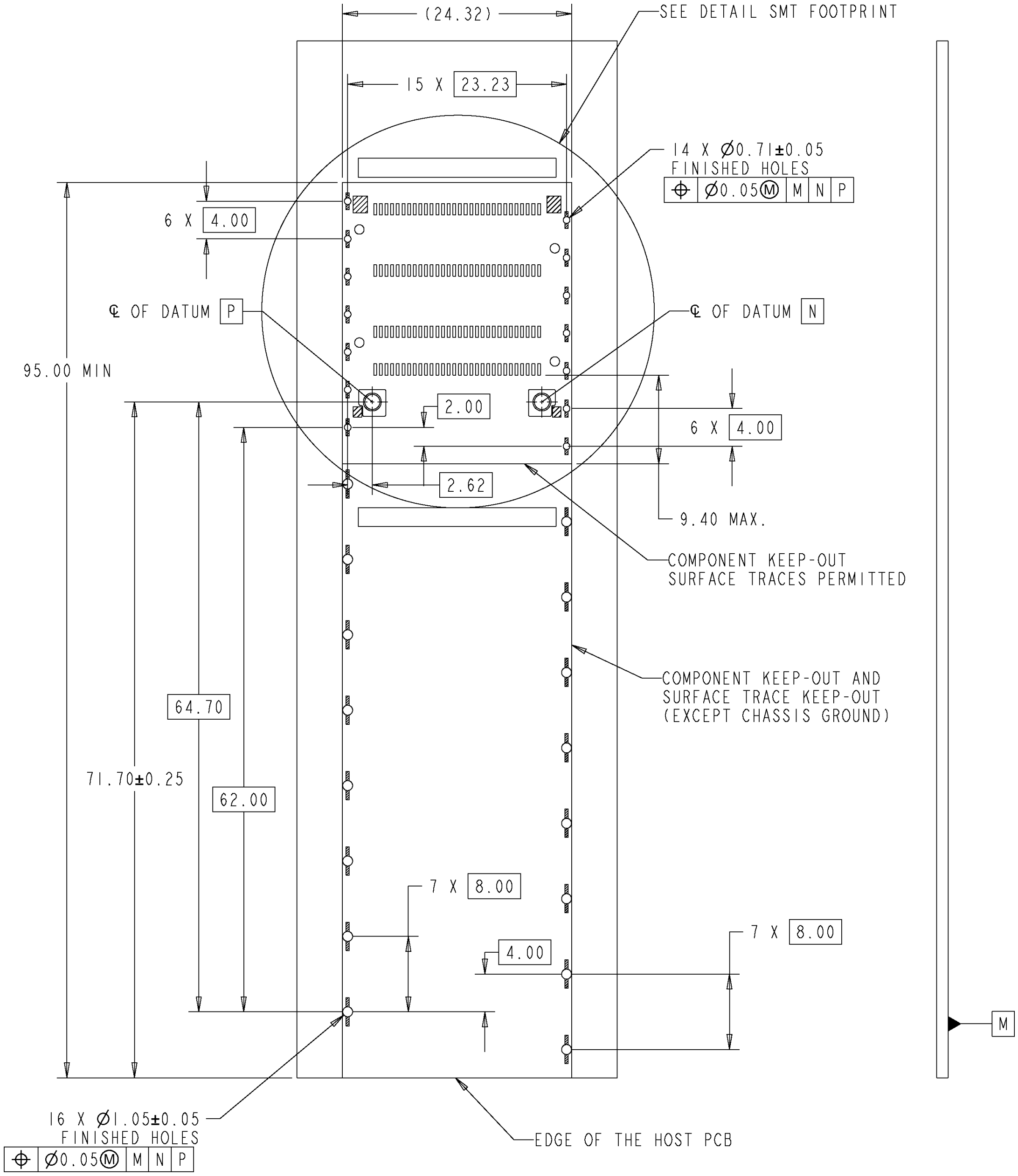


Figure 7-30: Host PCB Layout for 2x1 SMT cage

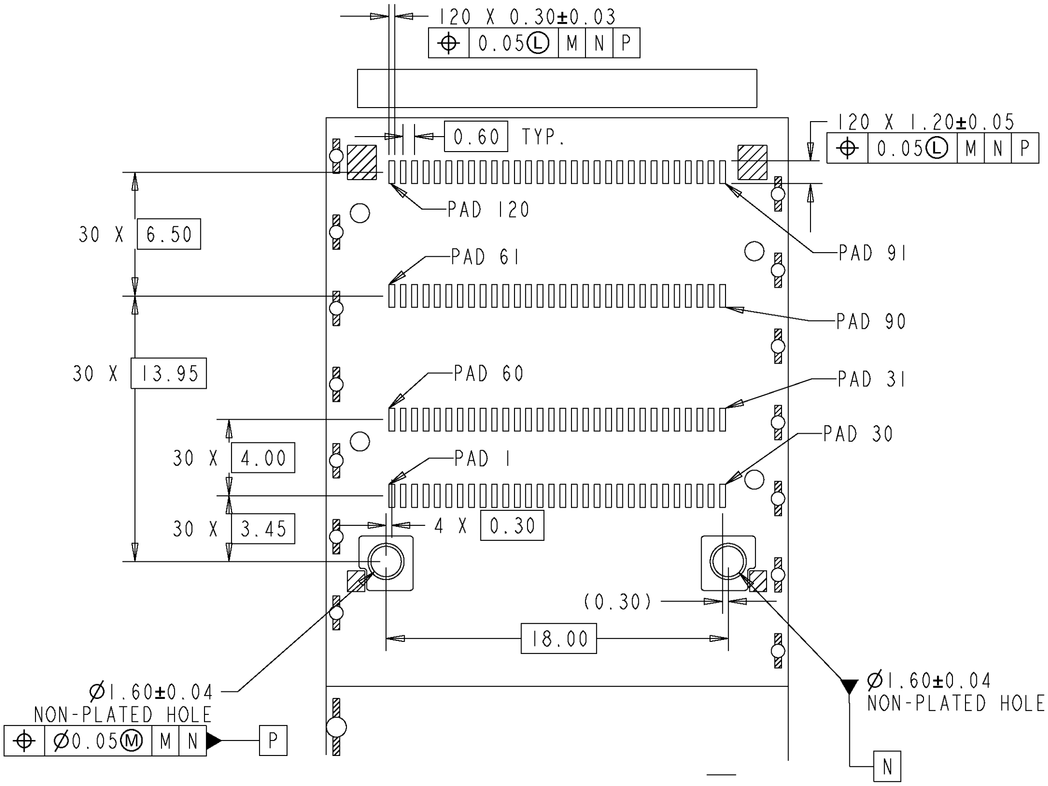


Figure 7-31: Host PCB layout, details

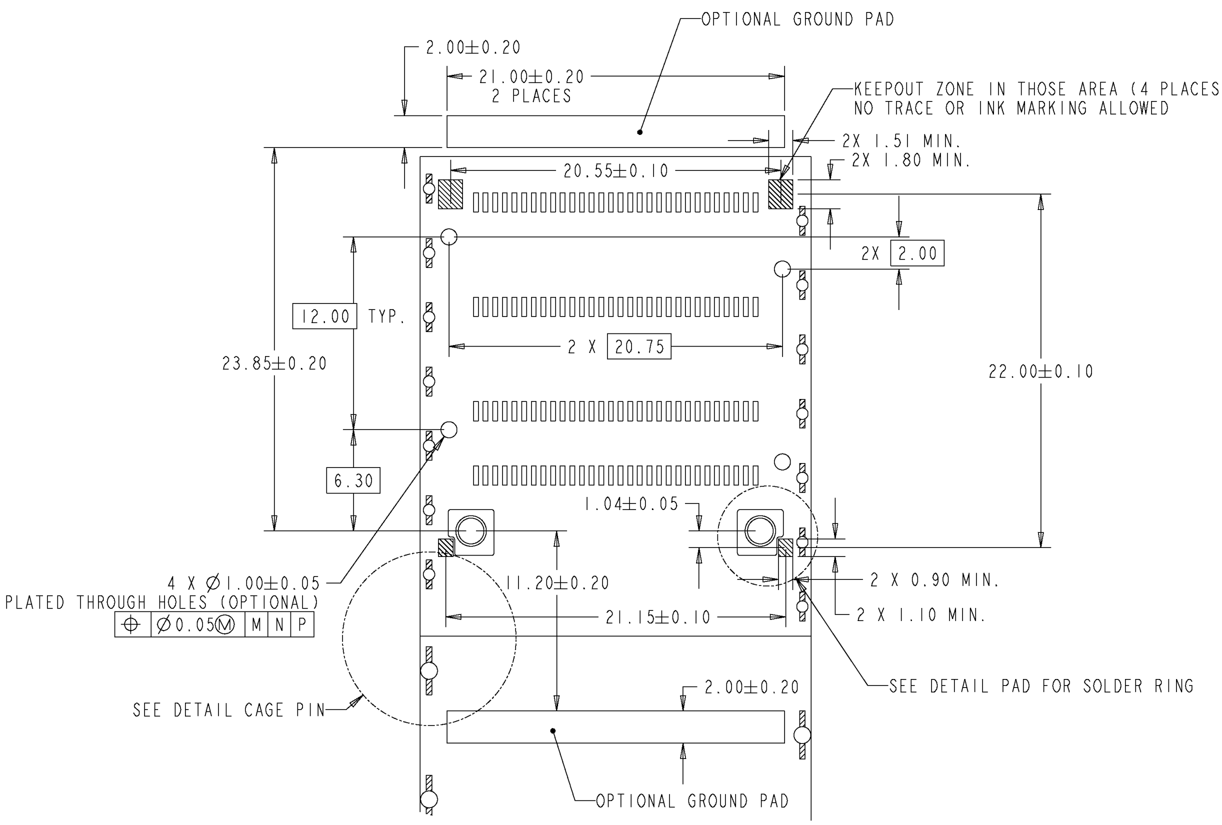


Figure 7-32: Layout for peg, retaining feature and ground pad

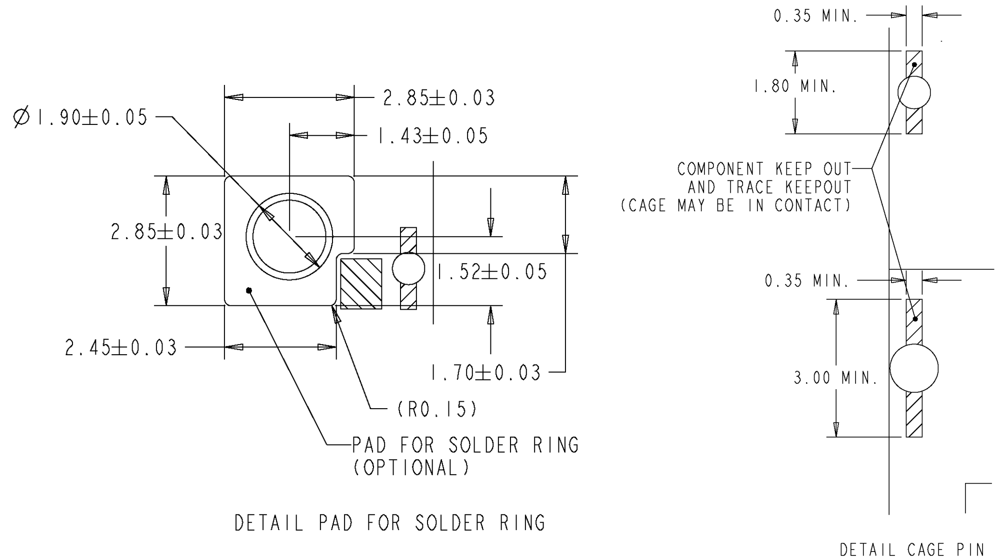


Figure 7-33: Details of pad for solder ring (left) and cage pin keepout (right)

7.5 Host PCB Layout – 2x4 Cage

In this section, host PCB layout for the ganged cage is presented in a 2x4 cage host layout. Figure 7-35 shows the comparison of 2x1, 2x2 and 2x4, while the detailed layout specification of the 2x2 is not provided here.

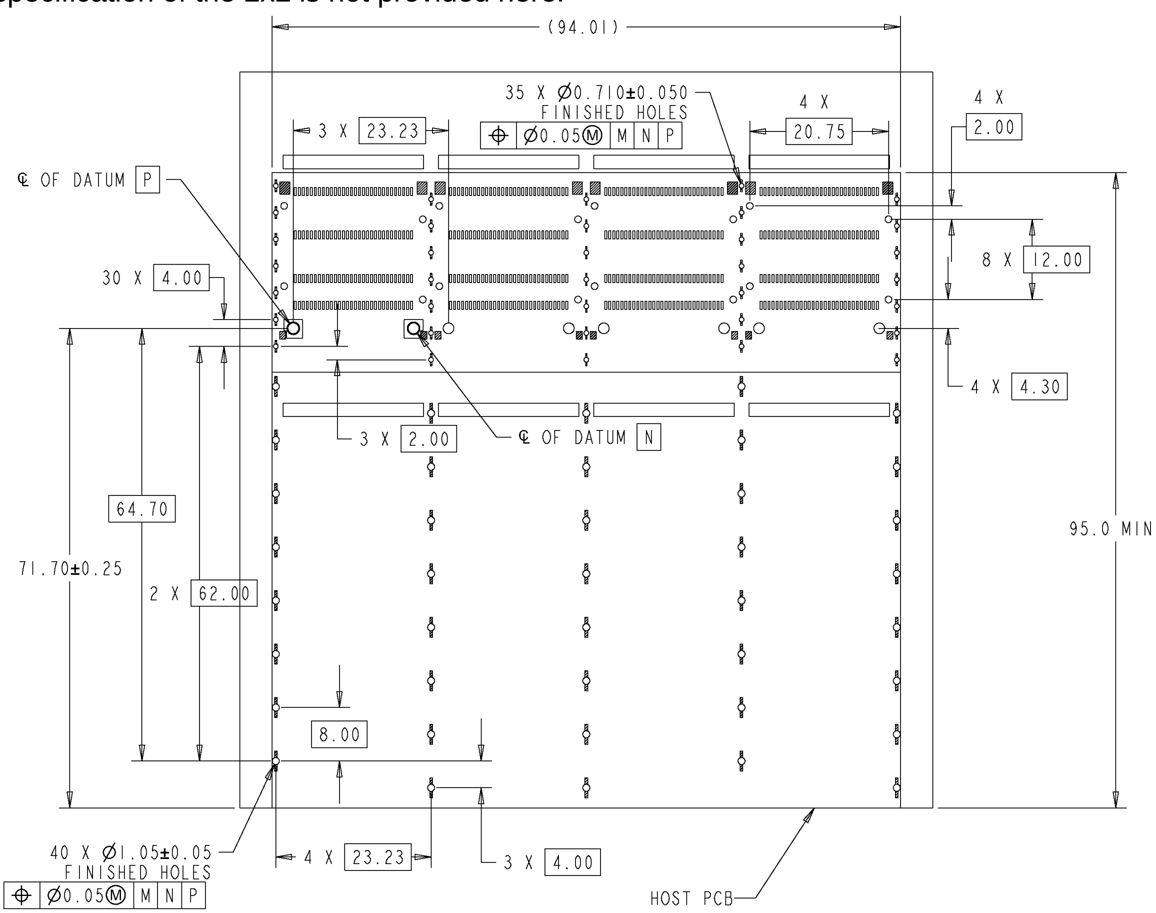


Figure 7-34: Host PCB layout for 2x4 cage

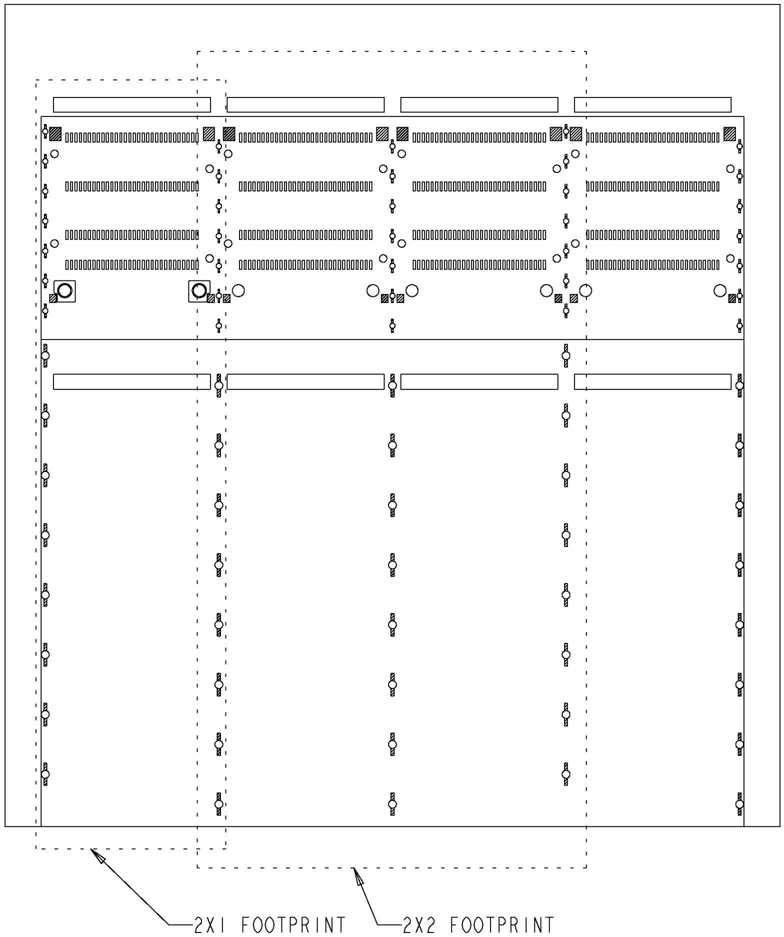


Figure 7-35: Comparison of SMT stacked 2x1, 2x2 and 2x4

7.6 PCB Thickness and Footprint for Belly-to-Belly Application

In this section, the minimum PCB thickness for the belly-to-belly application is shown, along with its host PCB layout. The cage and connector should be able to support a minimum PCB thickness as specified in Figure 7-6.

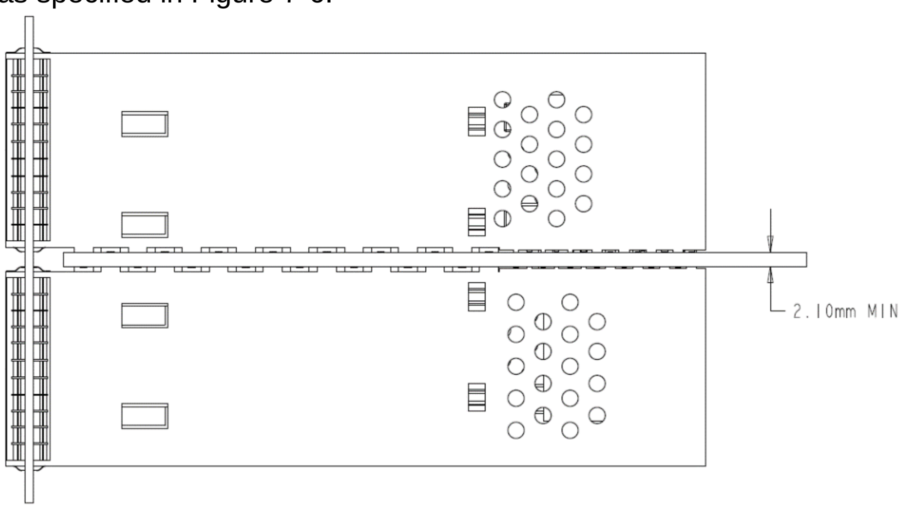


Figure 7-36: PCB thickness for belly-to-belly applications

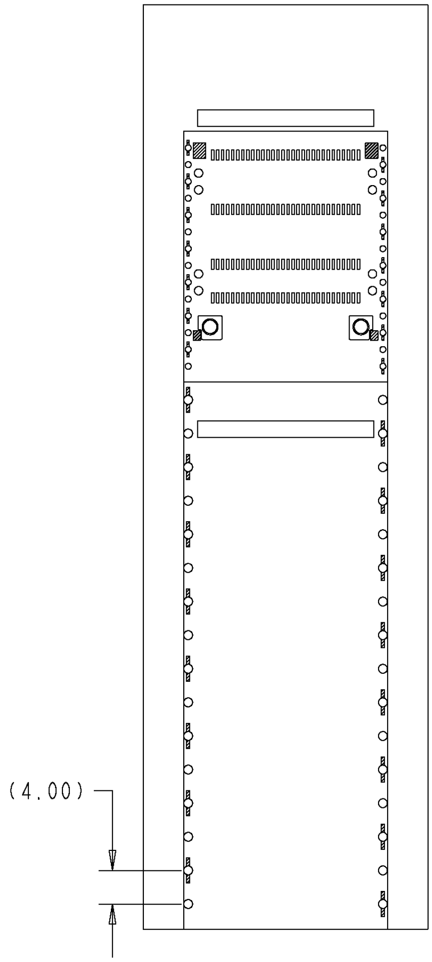


Figure 7-37: The host PCB layout for the 2x1 belly-to-belly applications

8 Press-fit Stacked OSFP Connector and Cage Mechanical Specification

In this section, the press-fit stacked connector and cage for OSFP is described. Note that the stacked SMT connector and cage is compatible only with Type 1 or Type 2 OSFP modules, not with Type 3 OSFP module as shown in Figure 3-3.

8.1 Overview

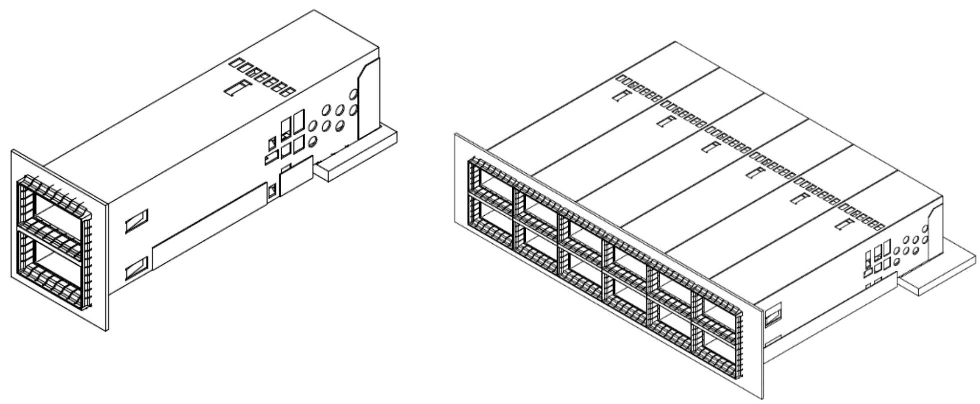


Figure 8-1: Overview of stacked cage, 2x1 and 2x6

In Figure 8-1, stacked cages of 2x1 and 2x6 are shown to demonstrate the stacked ganged cage. Both cages are shown with a host PCB and front panel.

For stacked cage, additional datum as defined in Table 8-1 shall apply.

Table 8-1: Descriptions of the module mechanical datum

Designator	Description	Figure
V	Centerline of the Connector Peg	Figure 8-15
Y	Rear Surface of the Connector	Figure 8-15

8.2 Cage Dimensions and Positioning Pin

Figure 8-2 shows the location of the cage positioning pins and the forward stop. Note that the host PCB have significant distance from the front of the cage. In Figure 8-3, the vertical pitch of the stacked cage is defined. To ensure sufficient strength of the cage compliant pins, two material thickness of 0.40mm and 0.25mm are used in the reference design of the cage. 0.40mm thickness is used where the cage compliant pins are used.

Figure 8-4 shows the reference dimensions of the cage when assembled with host PCB and OSFP module.

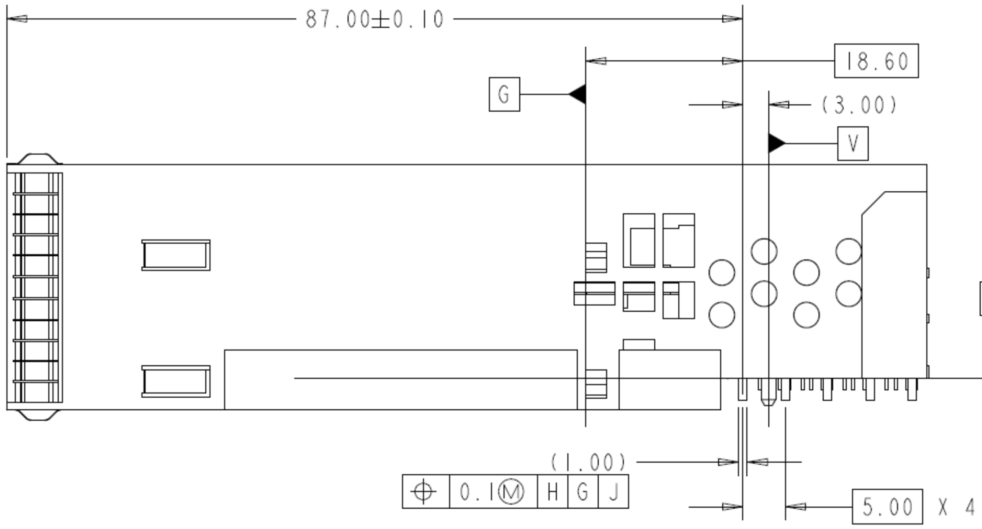


Figure 8-2: Stacked cage positioning pins and forward stop

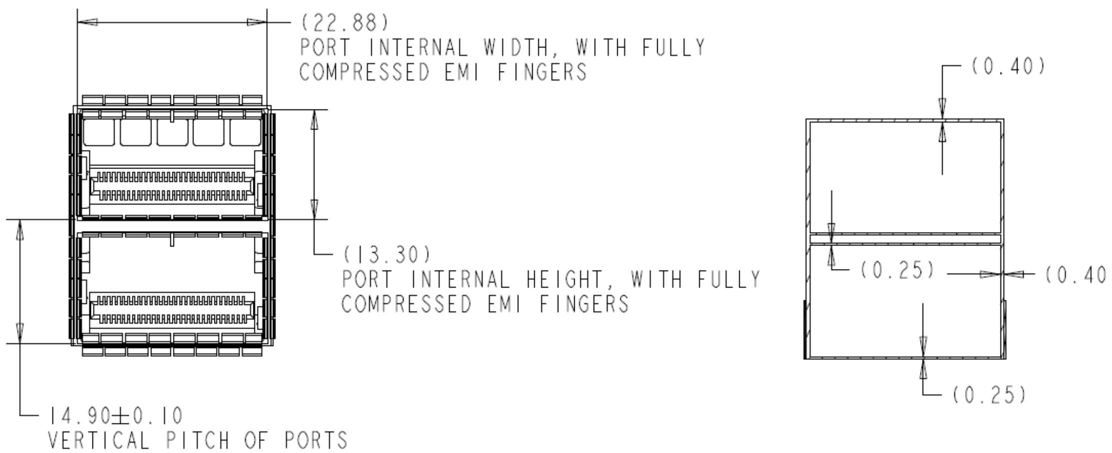


Figure 8-3: Stacked cage, port internal size, pitch and wall thickness

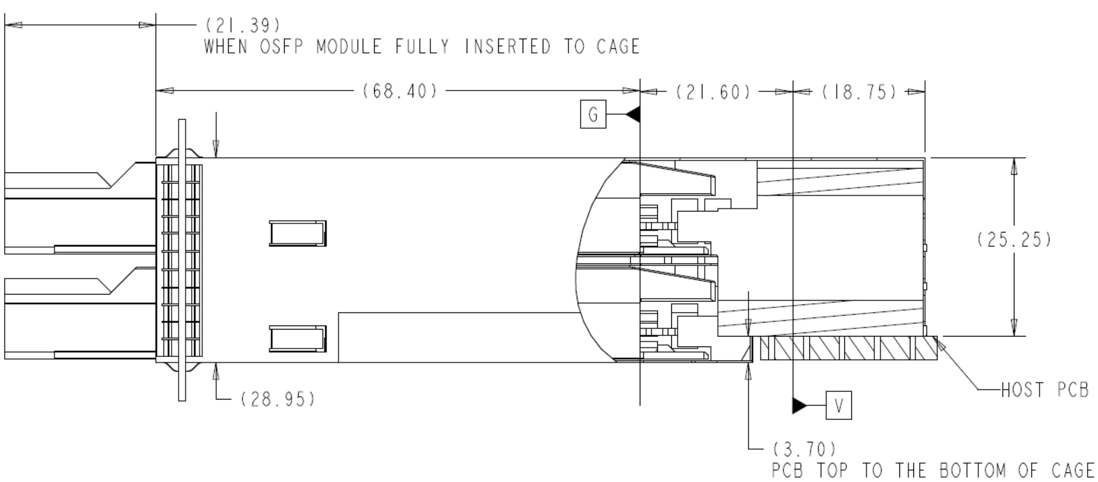


Figure 8-4: Cage with OSFP module, reference dimensions

8.3 Ventilation Holes

For proper cooling of the OSFP module in the stacked cage, the cage shall have appropriate ventilation holes. From Figure 8-5 to Figure 8-8, the ventilation holes required in the stacked ganged cage are described. The vent holes are designed not only to help with airflow from front to back of the cage, but also to help with airflow between the top and bottom rows of the cage, airflow between neighboring ports and to the bottom of the cage.

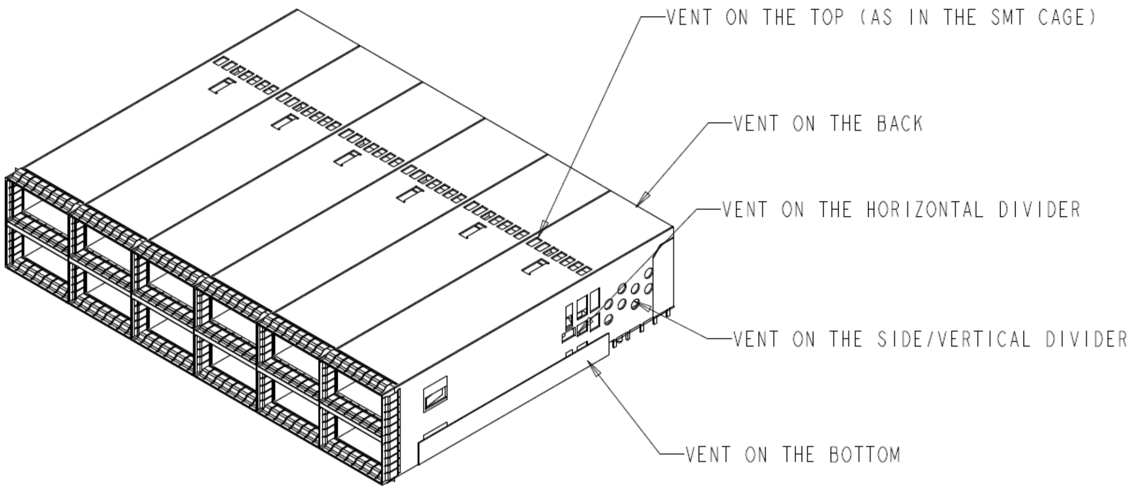


Figure 8-5: Overview of ventilation holes in the stacked cage

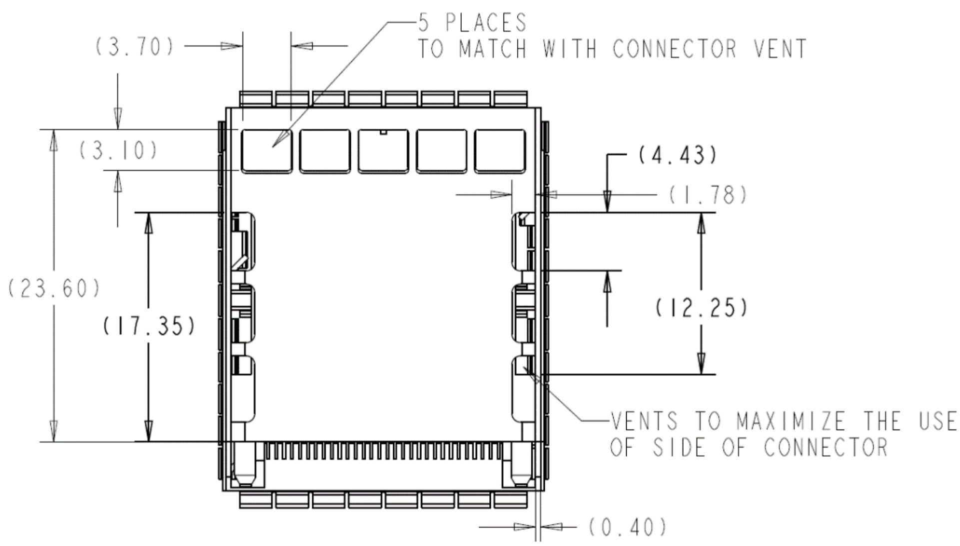


Figure 8-6: Ventilation holes at the back of the cage

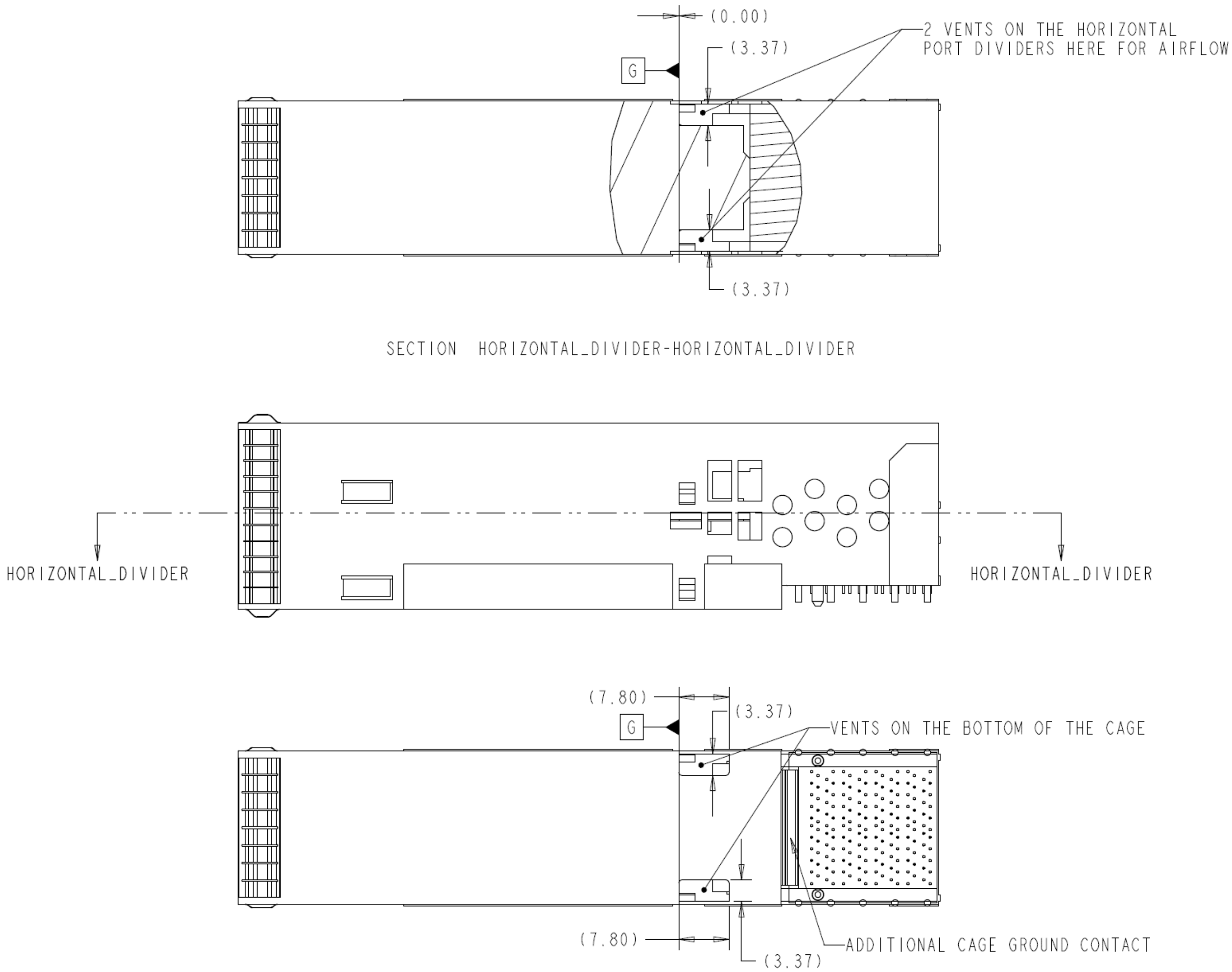


Figure 8-7: Ventilation holes in the horizontal divider and bottom

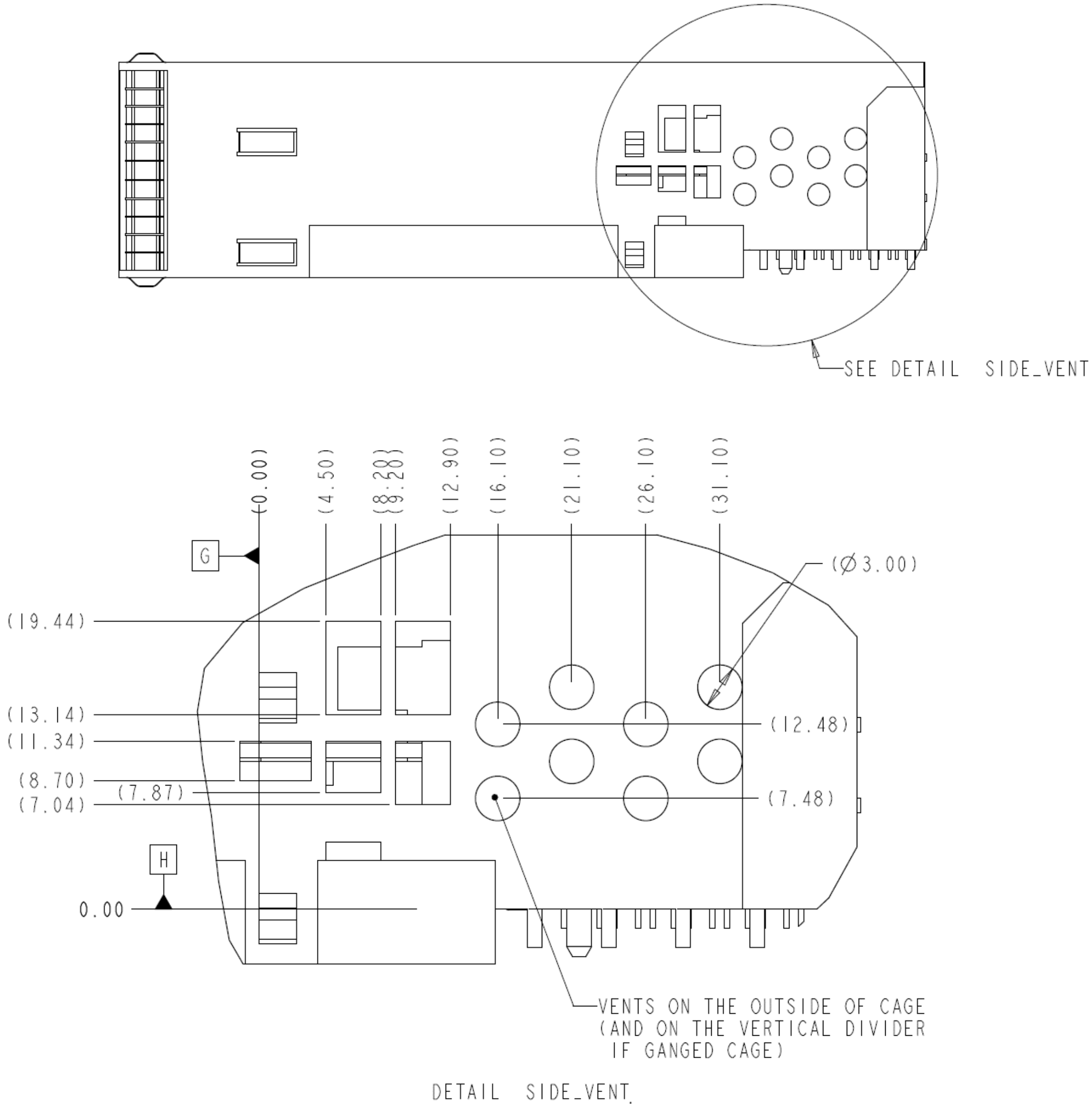


Figure 8-8: Ventilation holes in the side of the cage, and vertical divider

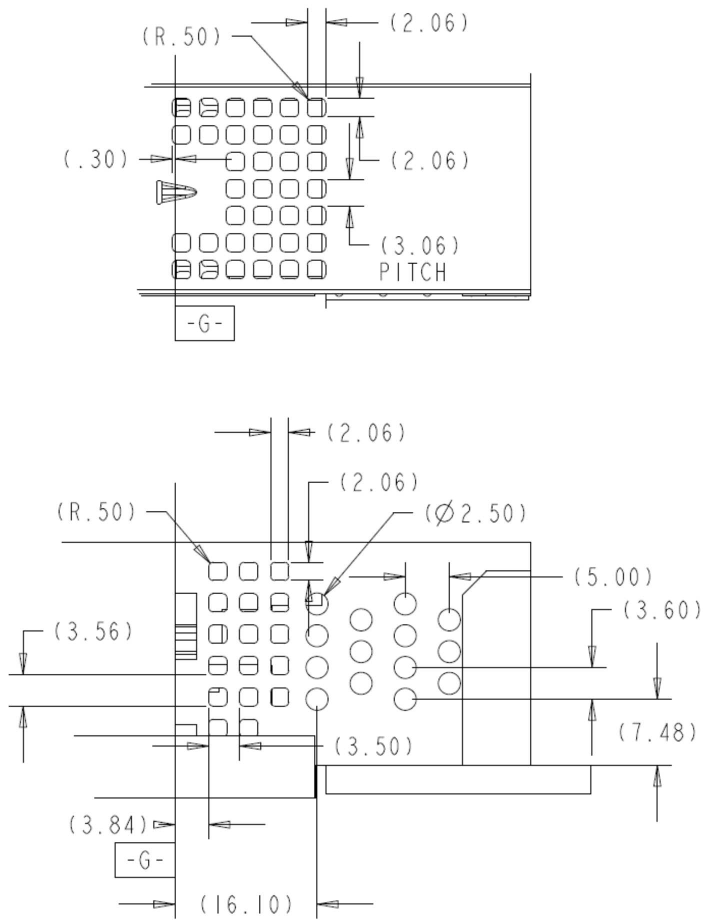
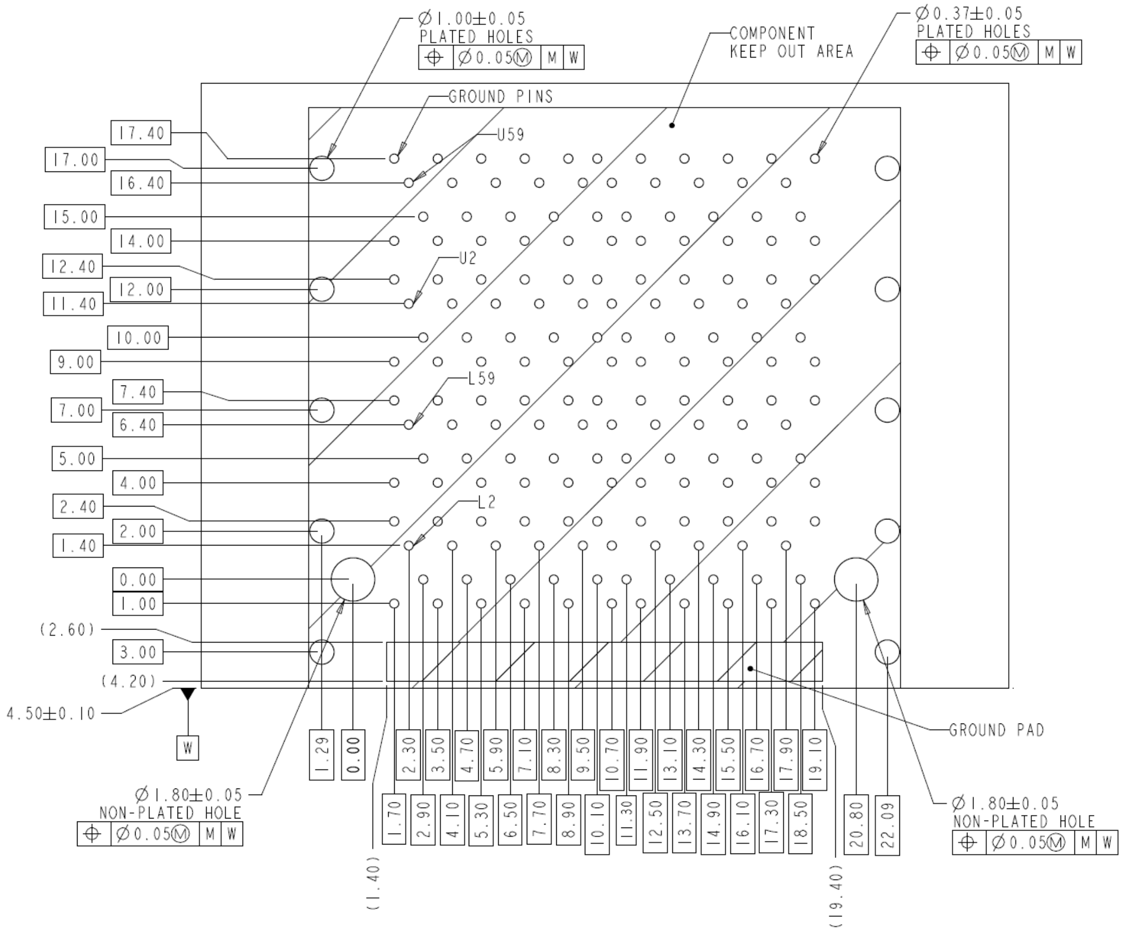


Figure 8-9: Ventilation holes in the top (above view) and side (bottom view) of the cage, alternative example

Rear ventilation pattern, Figure 8-6, is differ with stacked SMT cage in Figure 7-9 because the connector shapes are different. Figure 8-9 shows an alternative example design for top and side vent hole.

8.4 Host PCB Layout – 2x1 Cage



L2: PIN 2 OF THE LOWER PORT. U59: PIN 59 OF THE UPPER PORT.
SEE OSFP MODULE PIN OUT FOR PIN NUMBER CODE AND DETAIL FIGURE.

Figure 8-10: Host PCB layout for stacked connector

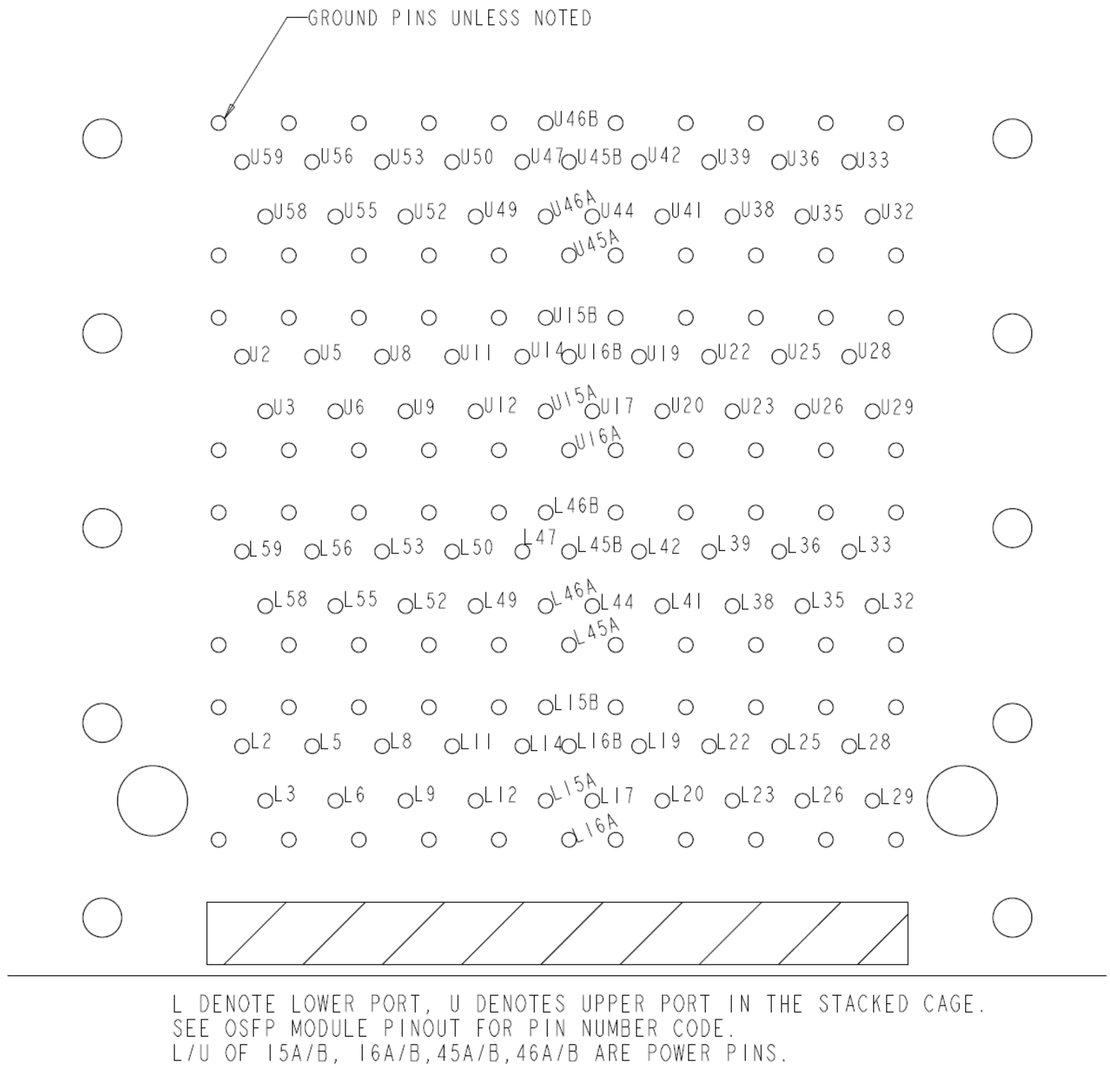


Figure 8-11: Host PCB pins for stacked connector

8.5 Host PCB Layout – Ganged Stacked Cage

As shown in the Figure 8-12, ganged stacked cages shall have a pitch of 23.38mm.

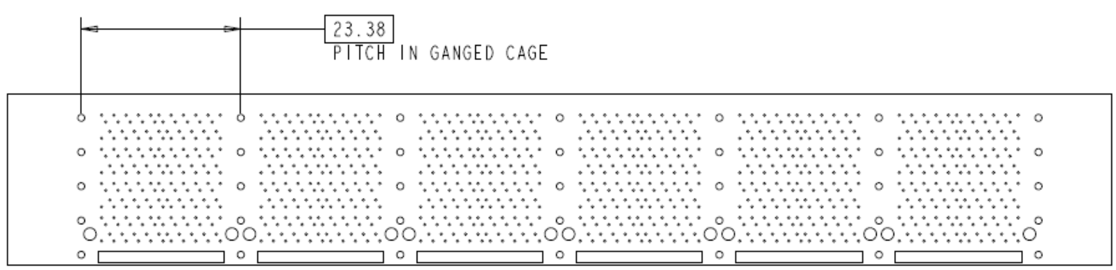


Figure 8-12: Host PCB layout for stacked ganged cage (shown with 2x6)

8.6 Bezel Panel Cut-out

Figure 8-13 shows the bezel cut out for a 2x1 cage. Figure 8-14 shows bezel cut out for a 2x6 cage.

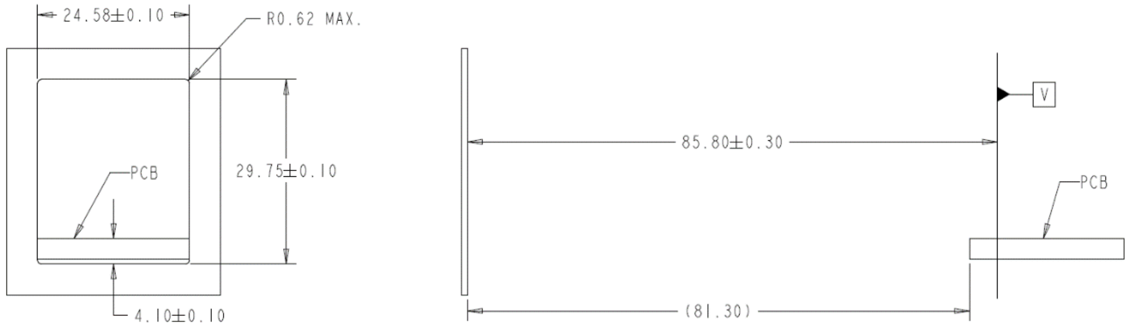


Figure 8-13: Bezel design and location for 2x1 cage

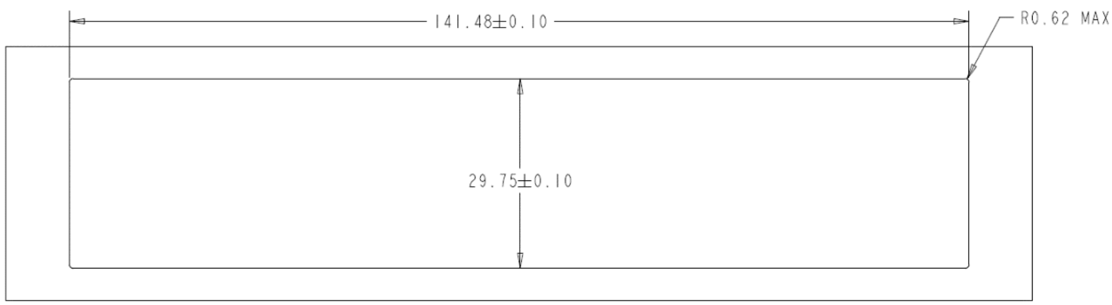


Figure 8-14: Bezel design for 2x6 cage

8.7 Electrical Connector for Stacked Cage (Press-fit)

The stacked electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module and be expelled outside.

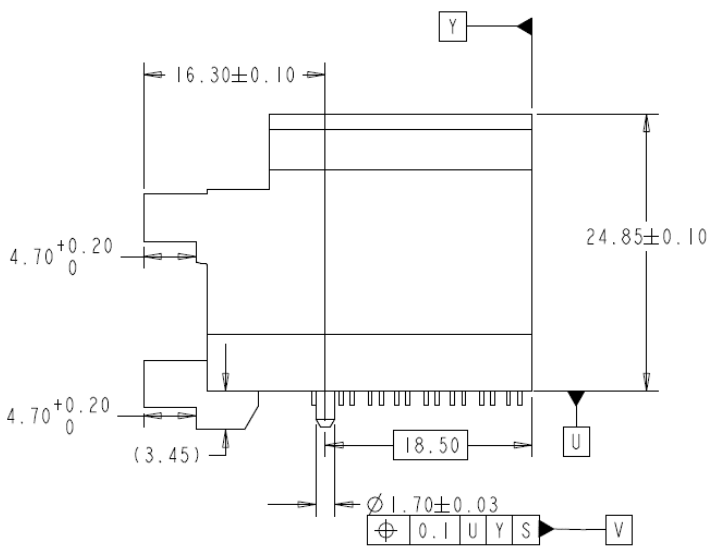


Figure 8-15: Stacked connector, side view

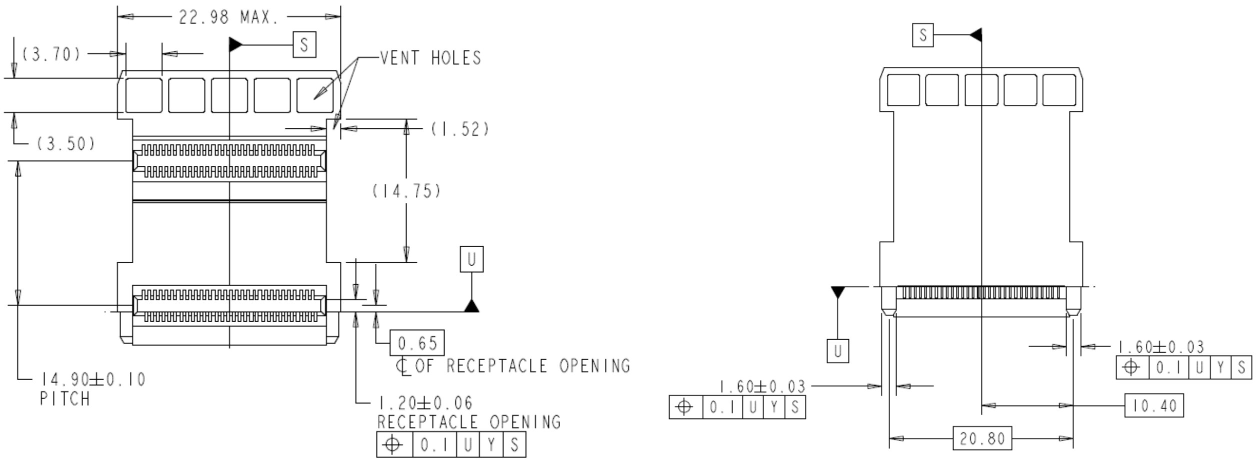


Figure 8-16: Stacked connector, front and back view

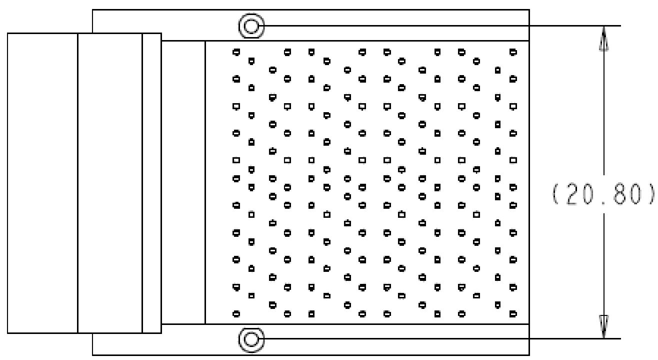


Figure 8-17: Stacked connector, bottom view

9 Cabled Connector Footprints

In this section, footprints for the cabled connectors are shown. Low speed signal and power are delivered through the host board and the compliance pin in the cabled connector, while the high speed signals will be transmitted through the cable.

The connector and the cage are not shown in this section but shall be compatible with all OSFP modules. The mechanical features of the connector and the cage will be compatible with the 1x1 SMT or 2x1 SMT connector and cage shown in the previous sections.

9.1 1x1 Cabled Host Footprint

For single side application, two types of host PCB footprints, CHF-A (Cabled Host Footprint A) and CHF-B, are available. See Figure 9-1 to Figure 9-4 for the details of those footprints.

Figure 9-5 and Figure 9-6 show CHF-B2B (Cabled Host Footprint for Belly to Belly), which is for belly to belly configuration for both sides with the cabled connectors. In CHF-B2B, one side is CHF-A and the other side is CHF-B to avoid interference.

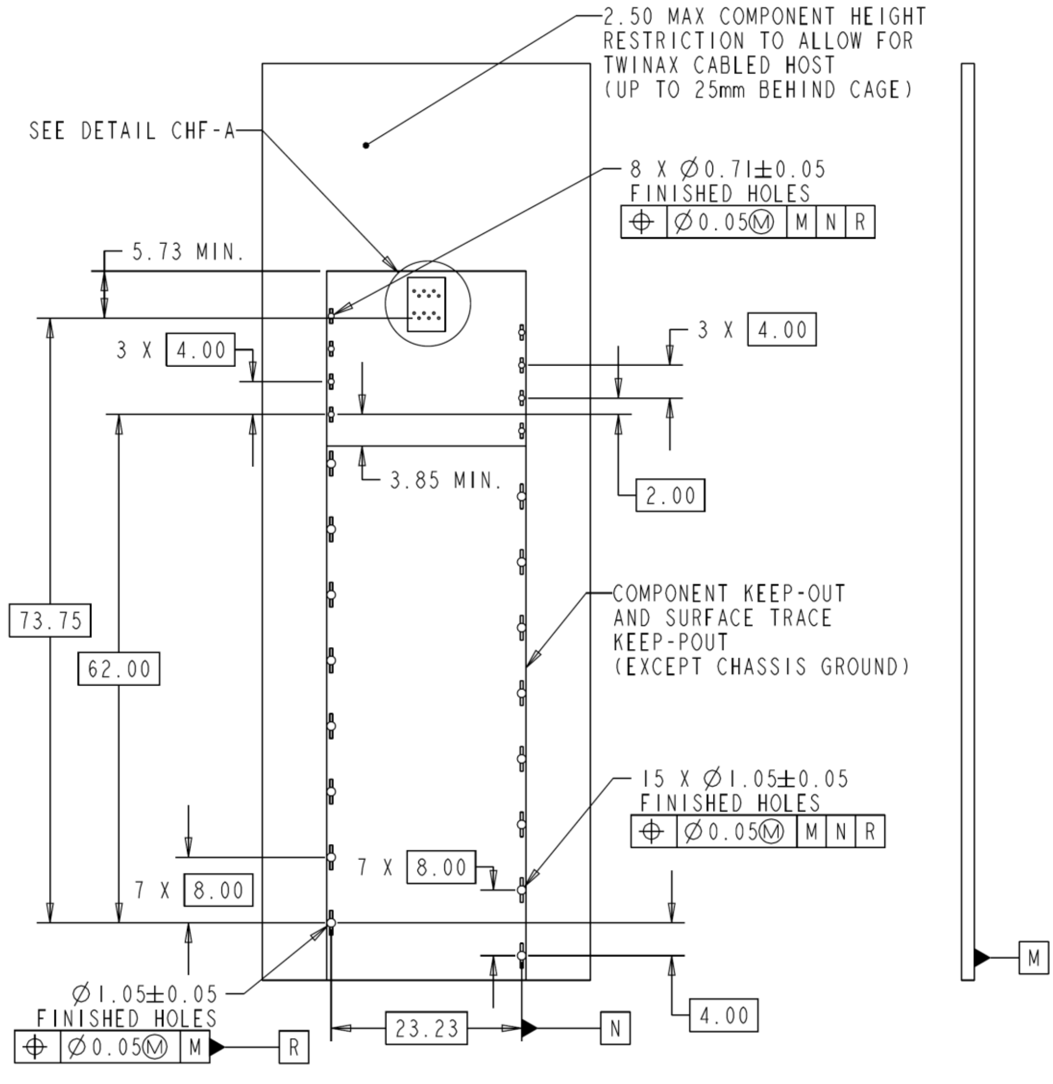


Figure 9-1: CHF-A (Cabled Host Footprint A)

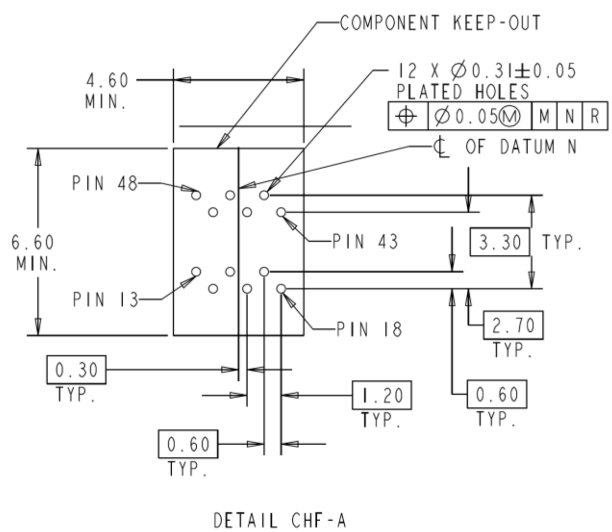


Figure 9-2: Detail of CHF-A

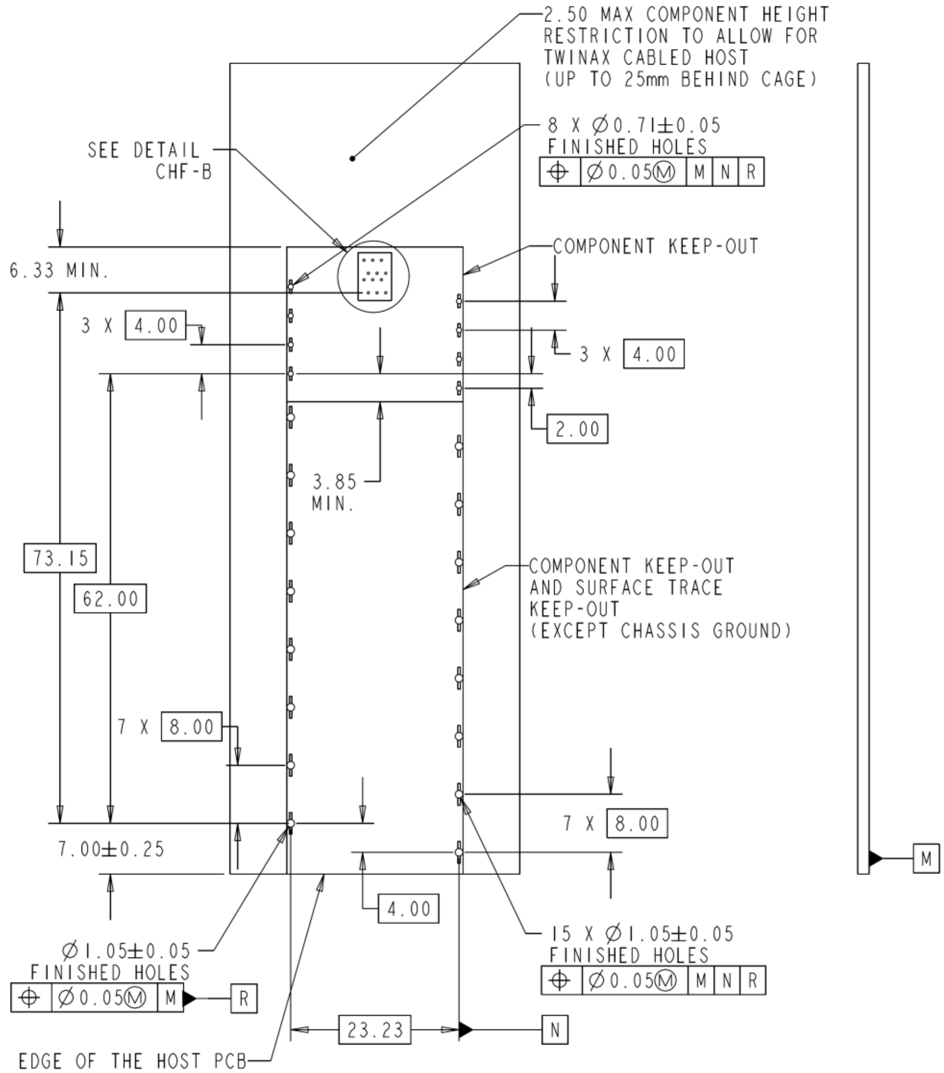


Figure 9-3: CHF-B (Cabled Host Footprint B)

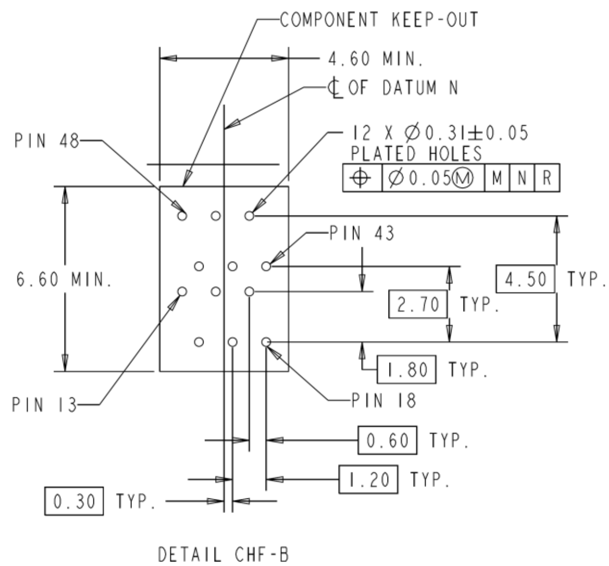


Figure 9-4: Detail of CHF-B

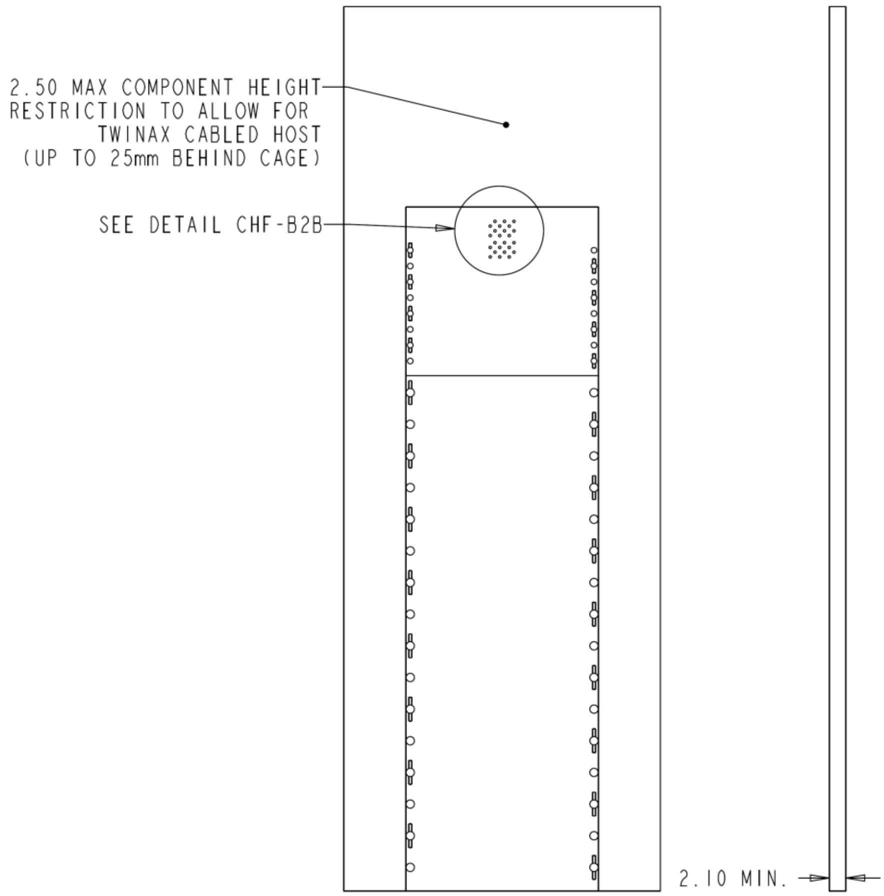


Figure 9-5: CHF-B2B (Cabled Host Footprint, Belly to Belly)

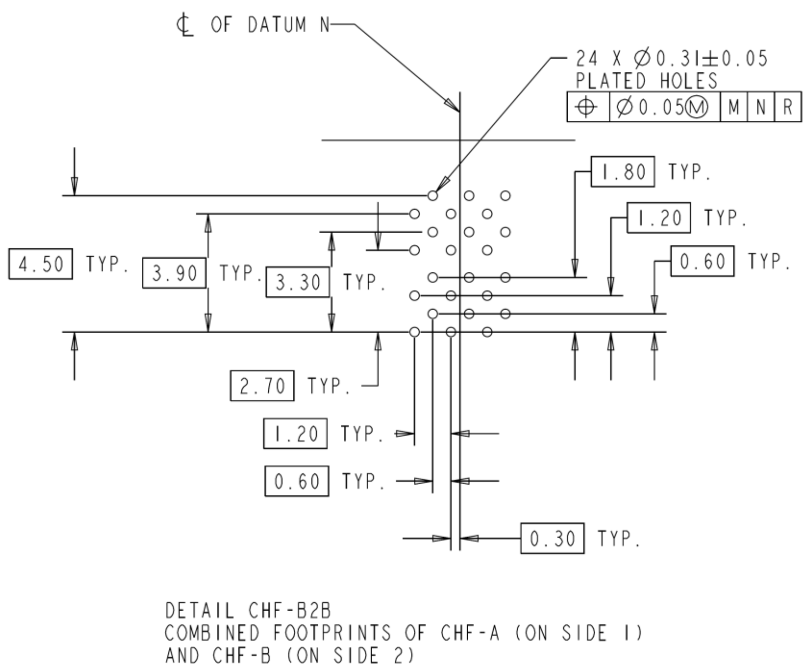


Figure 9-6: Detail CHF-B2B of the previous figure

Figure 9-7 and Figure 9-8 show the belly to belly footprint with single row SMT connector and the cabled connector on the other side. CHF-A is preferred as it gives more clearance from the plated through hole to the SMT soldering pads, as in the Figure 9-7.

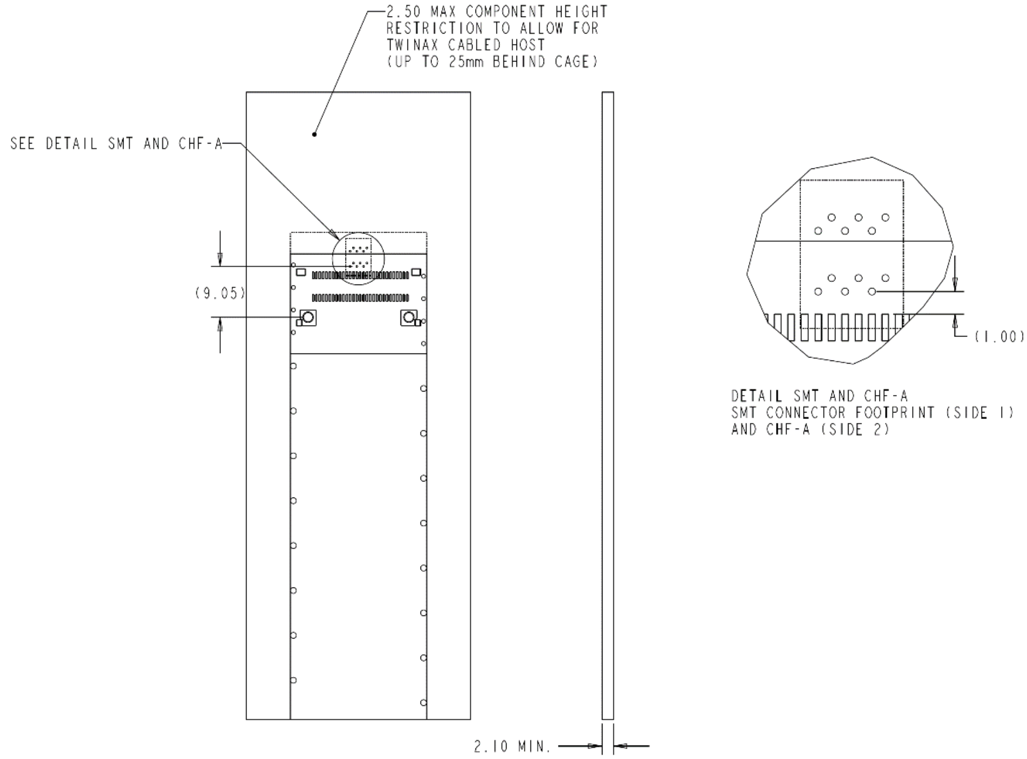


Figure 9-7: Belly to Belly, SMT and CHF-A

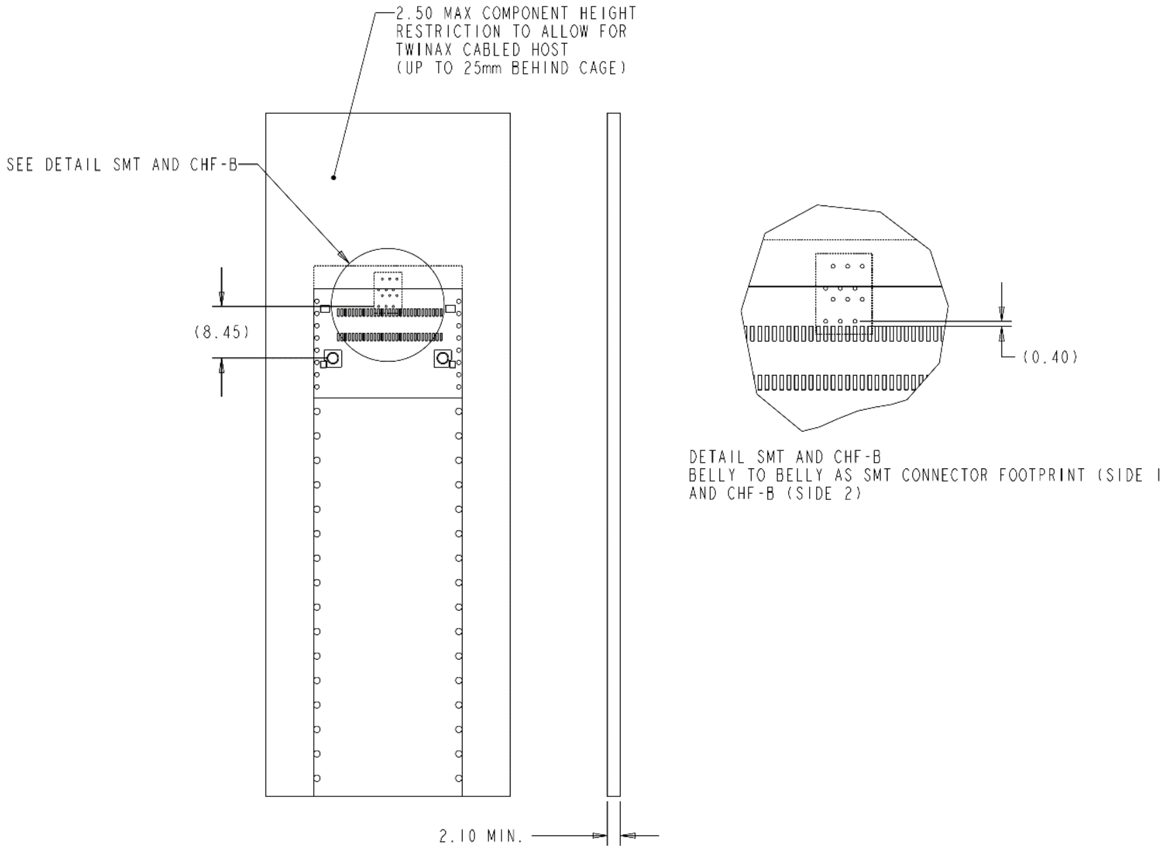


Figure 9-8: Belly to Belly, SMT and CHF-B

9.2 Host PCB Footprint, Stacked Cabled

In this section, host PCB footprint with stacked cabled connector and the cage is shown. There are two types in the footprint, 2x1 CHF-A and 2x1 CHF-B (Figure 9-9 to Figure 9-12) for single side application. For a belly to belly application, 2x1 CHF-B2B (Figure 9-13 and Figure 9-14) shall be used.

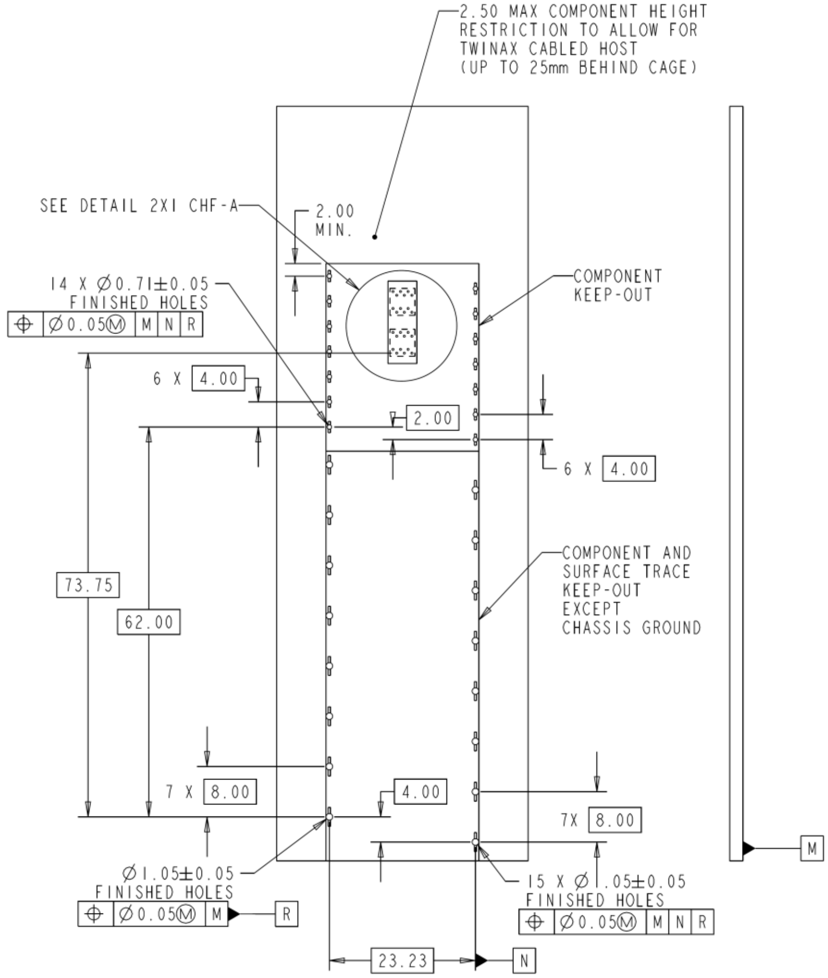


Figure 9-9: 2x1 CHF-A (2x1 Cabled Host Footprint A)

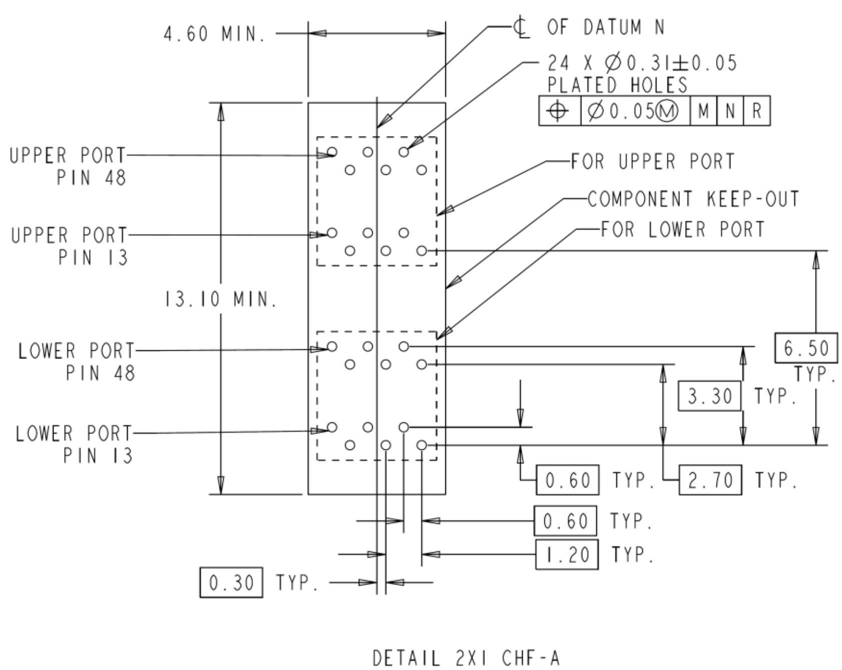


Figure 9-10: Detail of 2x1 CHF-A

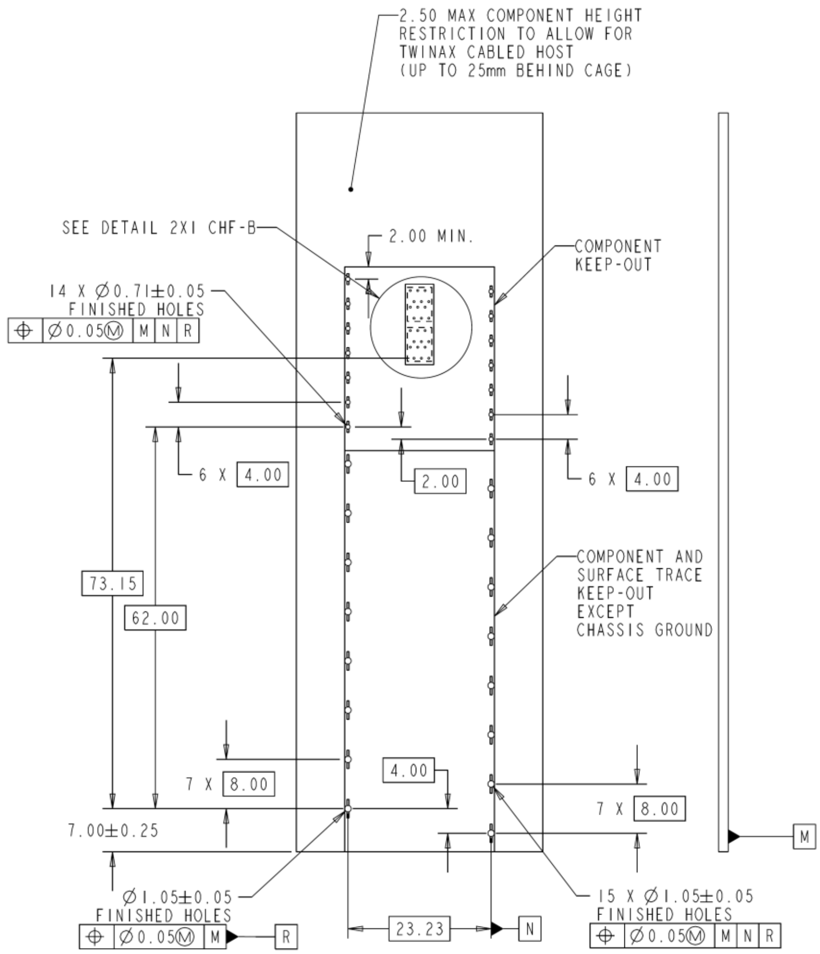


Figure 9-11: 2x1 CHF-B (2x1 Cabled Host Footprint B)

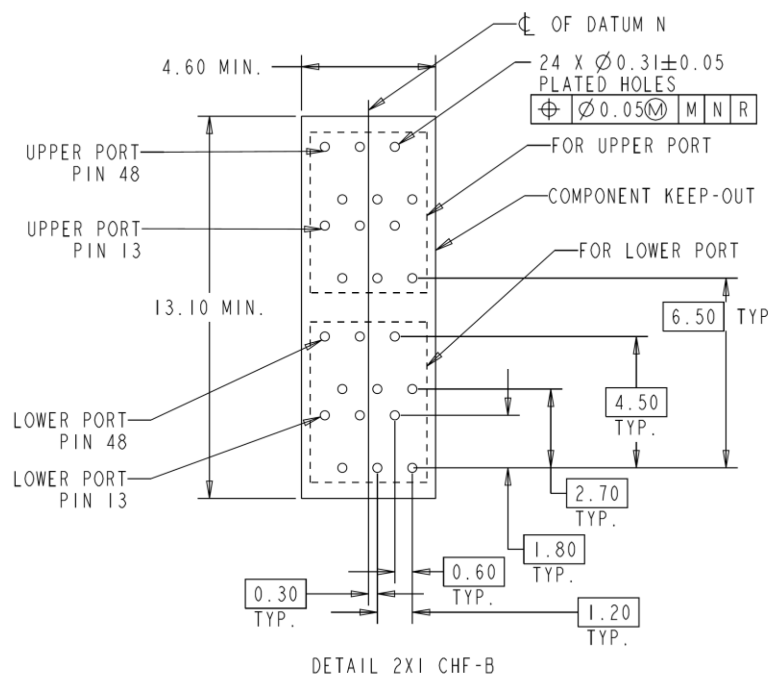


Figure 9-12: Detail of 2x1 CHF-B

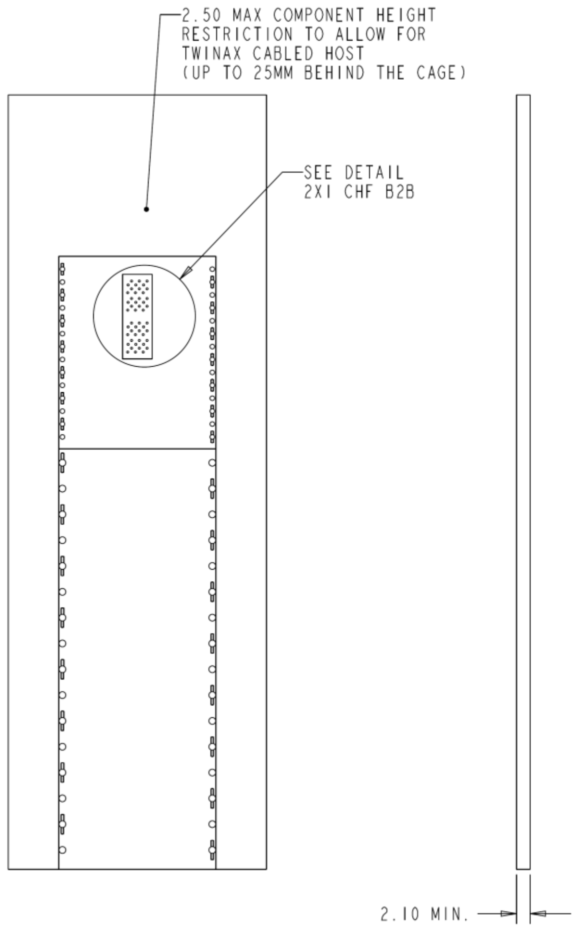


Figure 9-13: 2x1 CHF B2B (2x1 Cabled Host Footprint, Belly to Belly)

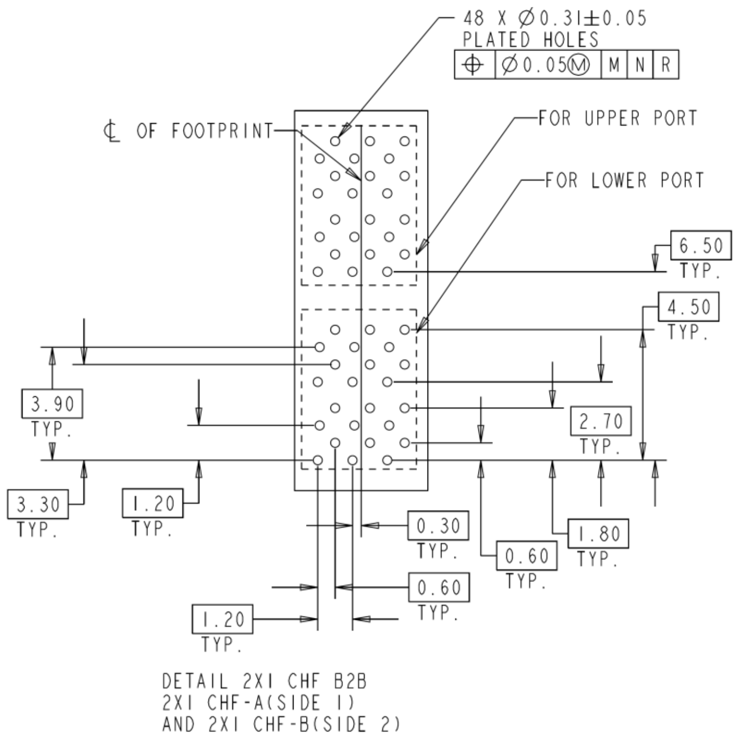


Figure 9-14: Detail of 2x1 CHF B2B

It is also possible to have a belly to belly of stacked SMT connector on one side of the board and the stacked cabled connector on the other side, as shown in the Figure 9-15. Although both type of the cabled connector can be used, 2x1 CHF-A is preferred as it gives more clearance between the footprints of both sides than 2x1 CHF-B.

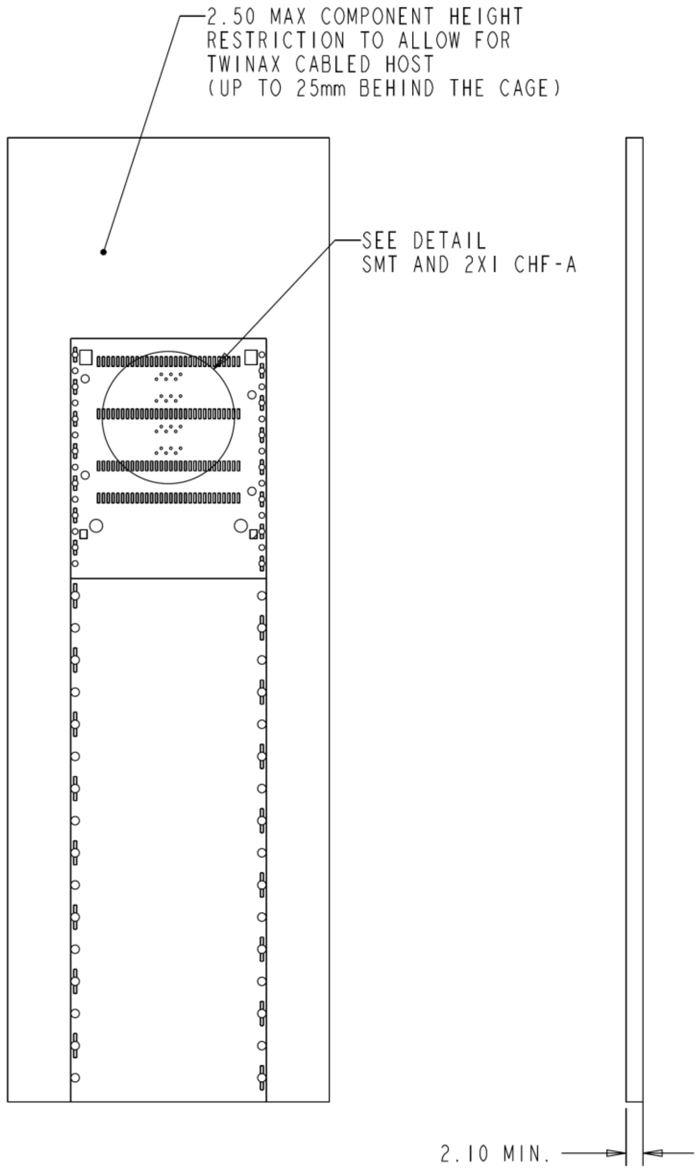


Figure 9-15: Belly to belly host footprint, top side stacked SMT and stacked cable B

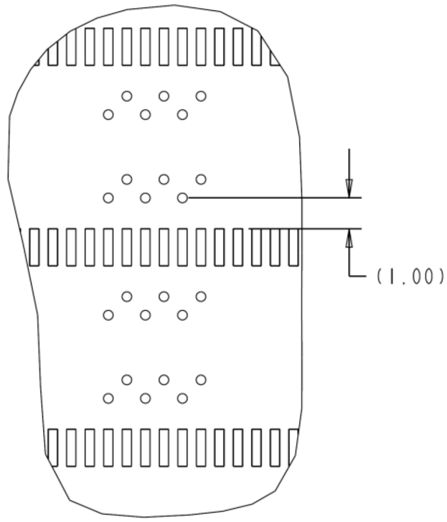


Figure 9-16: Detail 2x1 SMT-CABLED B of the previous figure

10 Plug-in and Removal of an OSFP Module

10.1 Insertion, Extraction, and Retention Forces for an OSFP Module

Table 10-1: Insertion, extraction, and retention forces for an OSFP module

Measurement	Minimum	Maximum	Units	Comments
OSFP Module Insertion	N/A	40 (55)	N	Module to be inserted into connector and cage with latch mechanism engaged. (55N if the cage has riding heatsink)
OSFP Module Extraction	N/A	30 (45)	N	Module to be removed from connector and cage with latching mechanism disengaged. (45N if the cage has riding heatsink)
OSFP Module Retention in Cage	125	N/A	N	No functional damage to module, connector, or cage with latching mechanism activated. If the module has a pull tab, the pull tab should be able to withstand up to 90N of the pulling under max operating temperature of the module.

10.2 Durability

The required number of insertion and removal cycles as applicable to the OSFP module, its mating connector, and cage are found in Table 10-2. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector, or cage.

Table 10-2: Durability

Insertion/Removal Cycles into Connector/Cage	Minimum (cycles)	Comments
Module Cycles	50	Number of cycles for an individual module, to be tested with cage, connector, and module; latches may be locked out during testing
Connector/Cage Cycles	100	Number of cycles for the connector and cage with multiple modules, to be tested with cage, connector, and module; latches may be locked out during testing

11 Thermal Performance

11.1 OSFP Module Thermal Requirements

The OSFP module shall operate within one or more of the case temperature ranges defined in Table 11-1. The temperature ranges are applicable between 60m below sea level and 1800m above sea level.

The module supplier is responsible for defining a location in the module where the case temperature can be measured or monitored. The location should be close to, and sufficiently thermally-coupled to, the component with the least thermal margin. See Appendix G for further details.

Table 11-1: Temperature range classes

Class	Case Temperature
Standard	0 through 70°C
Reduced	20 through 60°C
Extended	-5 through 85°C
Industrial	-40 through 85°C
Custom	Custom temperature range. Module shall be able to post temperature range to host via management interface.

Table 11-1 defines case temperature only. For reference, touch temperature is controlled by regulatory requirements for handling and incidental contact defined section 3.9.

11.2 OSFP Connector Thermal Requirements

The OSFP connector is required to achieve the following thermal requirements while sustaining maximum power as defined in section 14.6.

*Table 11-2: OSFP Connector Thermal Requirements**

Parameter	Value
Life Expectancy	10 years
Maximum Ambient Temperature	65 °C
Maximum Temperature Rise of connector when all signal and power contacts energized simultaneously	30 °C

* Tested per EIA-364-70

11.3 OSFP Module Airflow Impedance Curve

Figure 11-1 shows a typical airflow impedance range of an OSFP (module only) as measured along or through its heat sink. This typical range of airflow impedance can be used as a reference in an OSFP module's heat sink design and system design.

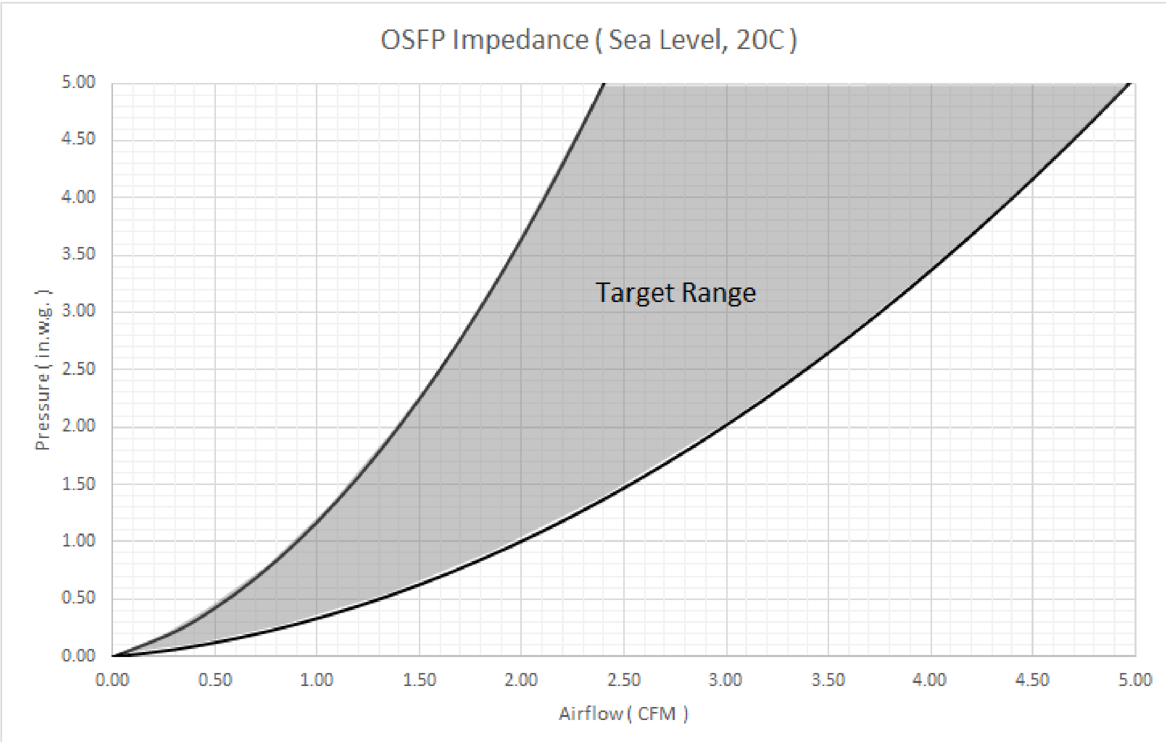


Figure 11-1: Target range of impediment to airflow of an OSFP module (20C, Sea Level)

11.4 Module Airflow Impedance Test Jig

The impedance range of Figure 11-1 was created using a jig as shown in Figure 11-2 and Figure 11-3. The jig is designed to support airflow along the heat sink as well as leakage around the module. The positive stop located within the jig reproduces the assembled condition within a host port. For a Type 2 or Type 3 module, the module will protrude beyond the jig opening.

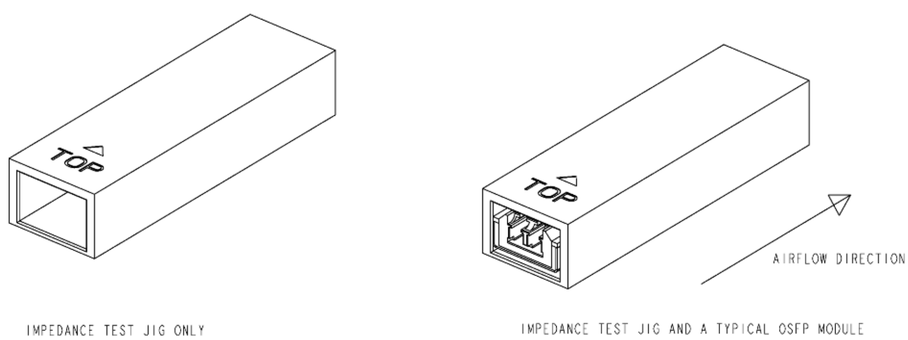


Figure 11-2: Impedance test setup for Type 1 and Type 2 OSFP module (Shown with Type 1)

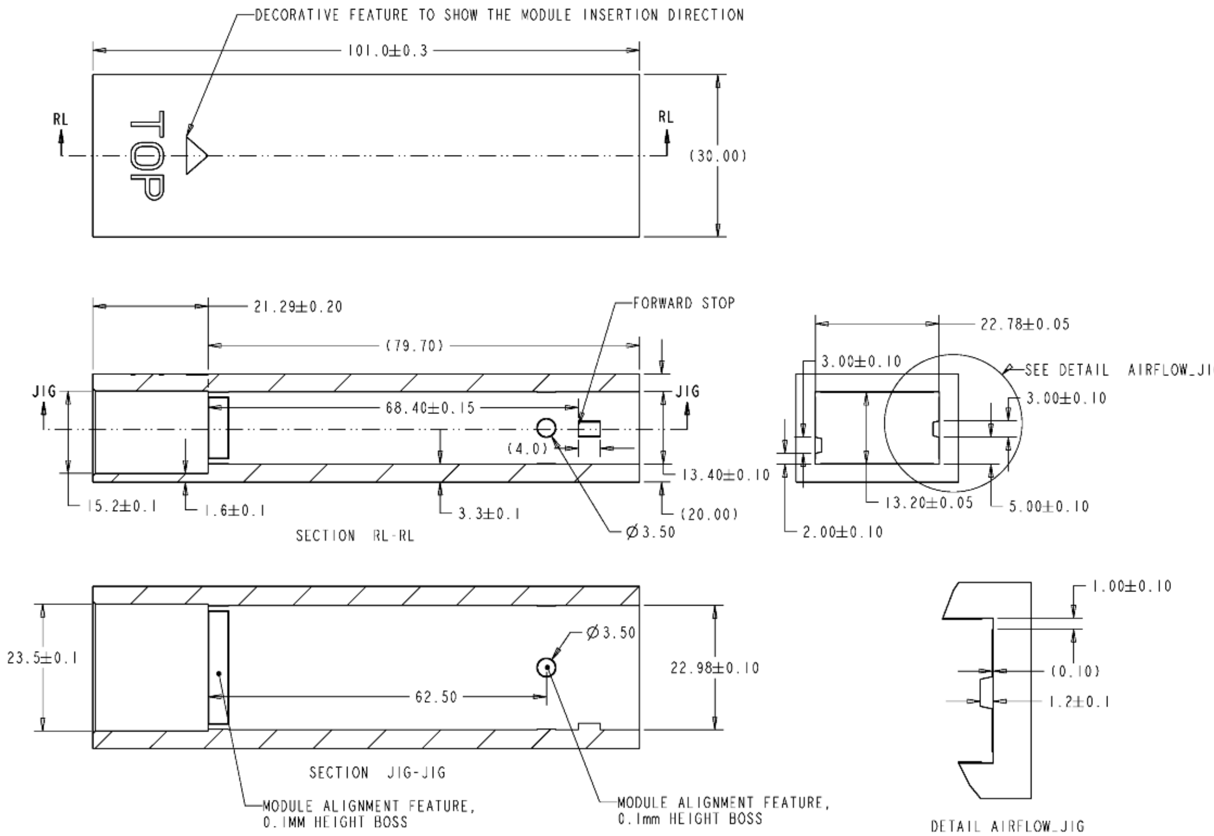


Figure 11-3: Impedance test jig for Type 1 and Type 2 OSFP

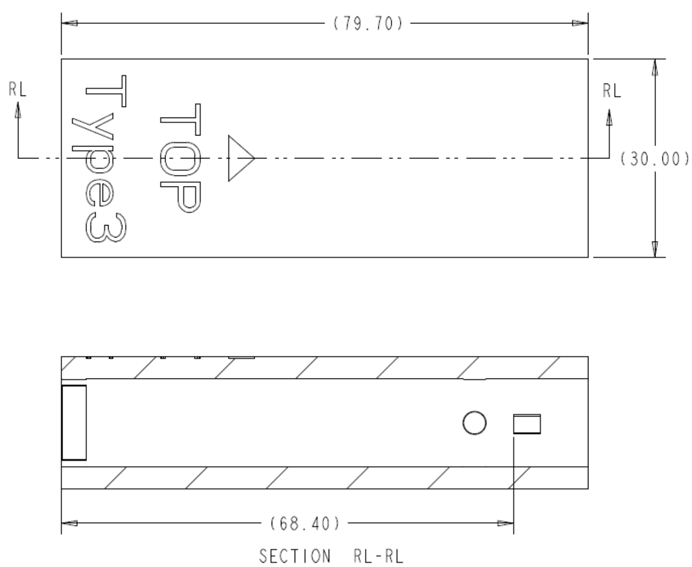


Figure 11-4: Impedance test jig for Type 3 OSFP

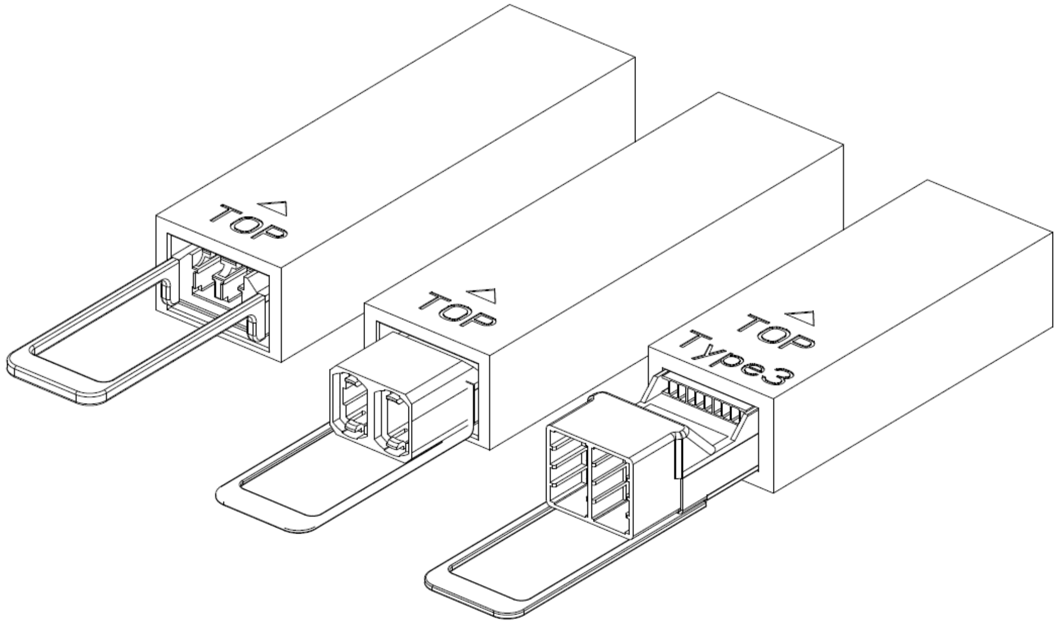


Figure 11-5: Impedance test setup for Type 1, Type 2 and Type 3 OSFP

12 OSFP Riding Heat Sink Module and Cage Mechanical Specification

12.1 Overview

OSFP Riding Heat Sink (OSFP-RHS) is a 9.5mm tall pluggable module which does not have an integrated heat sink as shown in the Figure 12-1 and Figure 12-2. In place of OSFP's integrated heat sink, OSFP-RHS cage shall have a riding heat sink. To prevent insertion of OSFP-RHS into a standard OSFP cage, the shape and location of the positive stop has been changed. See Table 12-1 for a comparison between the OSFP-RHS and OSFP.

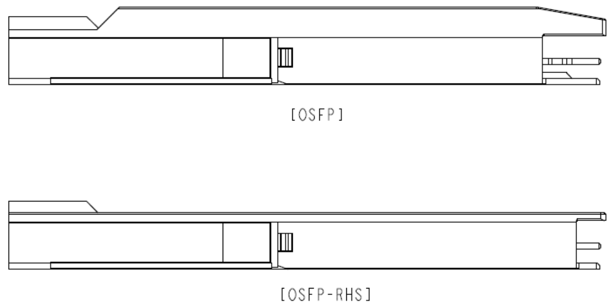


Figure 12-1: Side view of a typical OSFP (top) and a typical OSFP-RHS (bottom)

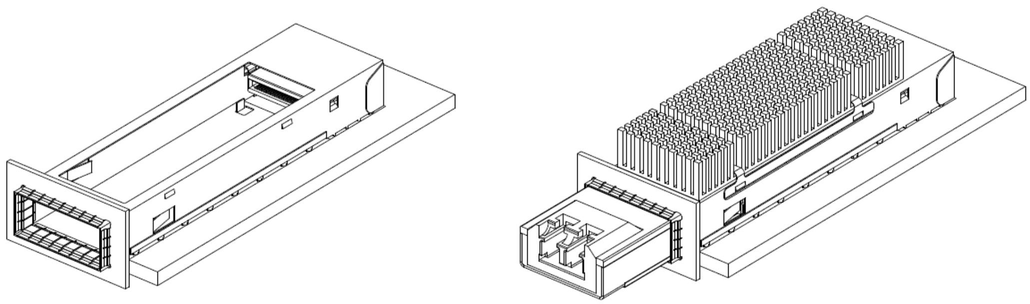


Figure 12-2: OSFP-RHS cage only (left) and OSFP-RHS cage with module and riding heat sink (right)

Table 12-1: Comparison of OSFP-RHS to OSFP

OSFP-RHS feature	Comment
Module	9.5mm height without heat sink and different positive stop; for the feature not explicitly specified for OSFP-RHS, the same specifications as OSFP shall be applied.
Connector	Identical with Surface Mount Connector
Host PCB Board Layout	Identical with Surface Mount type
Cage	Port height/positive stop/bezel cutout is different with OSFP
Insertion/Extraction/Retention	No change; see Table 10-1
Durability	Identical with OSFP
Thermal Requirement	Identical with OSFP
Airflow Requirement	Not applicable (Section 11.2 is not applied)
Electrical and Management interface	Identical with OSFP

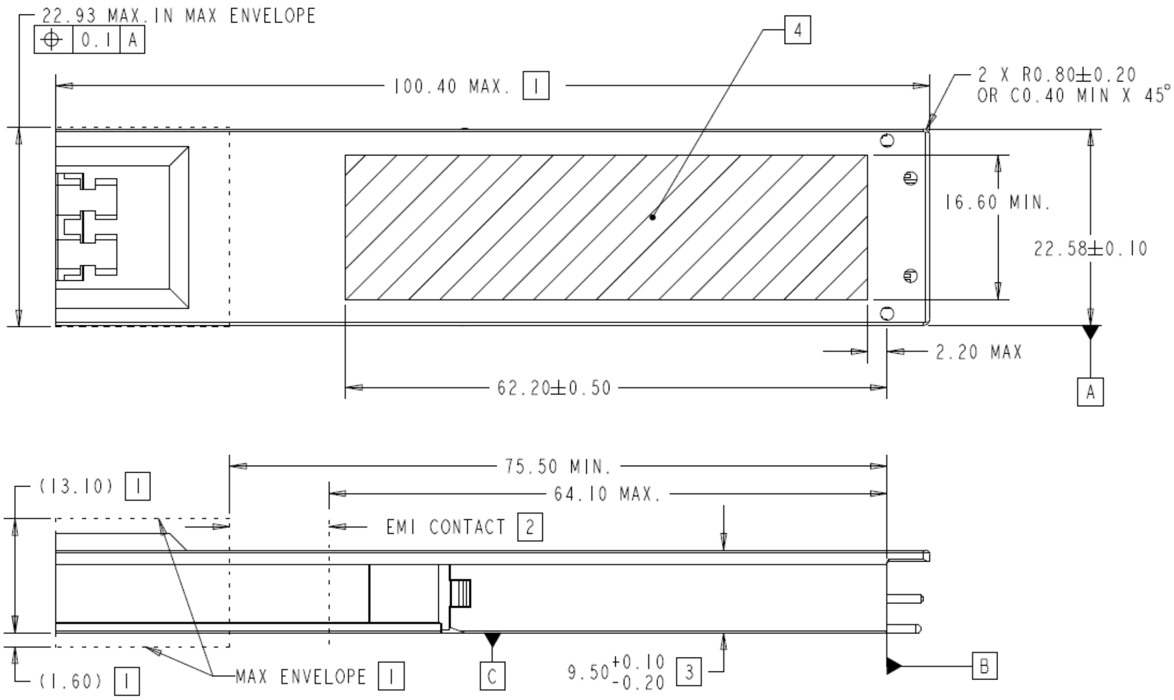
In the following sections, the dimensions of the OSFP-RHS will be defined.

As with the OSFP, OSFP1600-RHS supports 200G per lane, while OSFP-RHS or OSFP800-RHS supports 50G or 100G per lane. OSFP1600-RHS should follow section 12.4, while OSFP-RHS or OSFP800-RHS can either follow section 12.3 or section 12.4.

12.2 OSFP-RHS Module Mechanical Specification

Figure 12-3 shows the overall dimension of an OSFP-RHS module from a top view. The reference datum definition is identical to Table 3-1, but note that the location of the datum B (forward stop of the module) is shifted 6mm to prevent an OSFP-RHS from being fully inserted into an OSFP cage as described in section 4 or 5.

As in the OSFP and Figure 3-3, OSFP-RHS can be either Type 1, 2 or 3. Type 1, 2 and 3 are differ only in the max envelope of the module front, which are same envelope with each matching types of the OSFP. Figure 12-3 is showing type 1, and Figure 12-4 is showing type 1, 2 and 3.



NOTES:

1. MAX ENVELOPE OF THE FRONT OF THE MODULE WILL DIFFER BY MODULE TYPE. SHOWN WITH TYPE 1 MODEL.
2. INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
3. APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.
4. SURFACE TO BE THERMALLY CONDUCTIVE. REFER SECTION 12.5 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

Figure 12-3: Overview of the OSFP-RHS and heat sink contact area

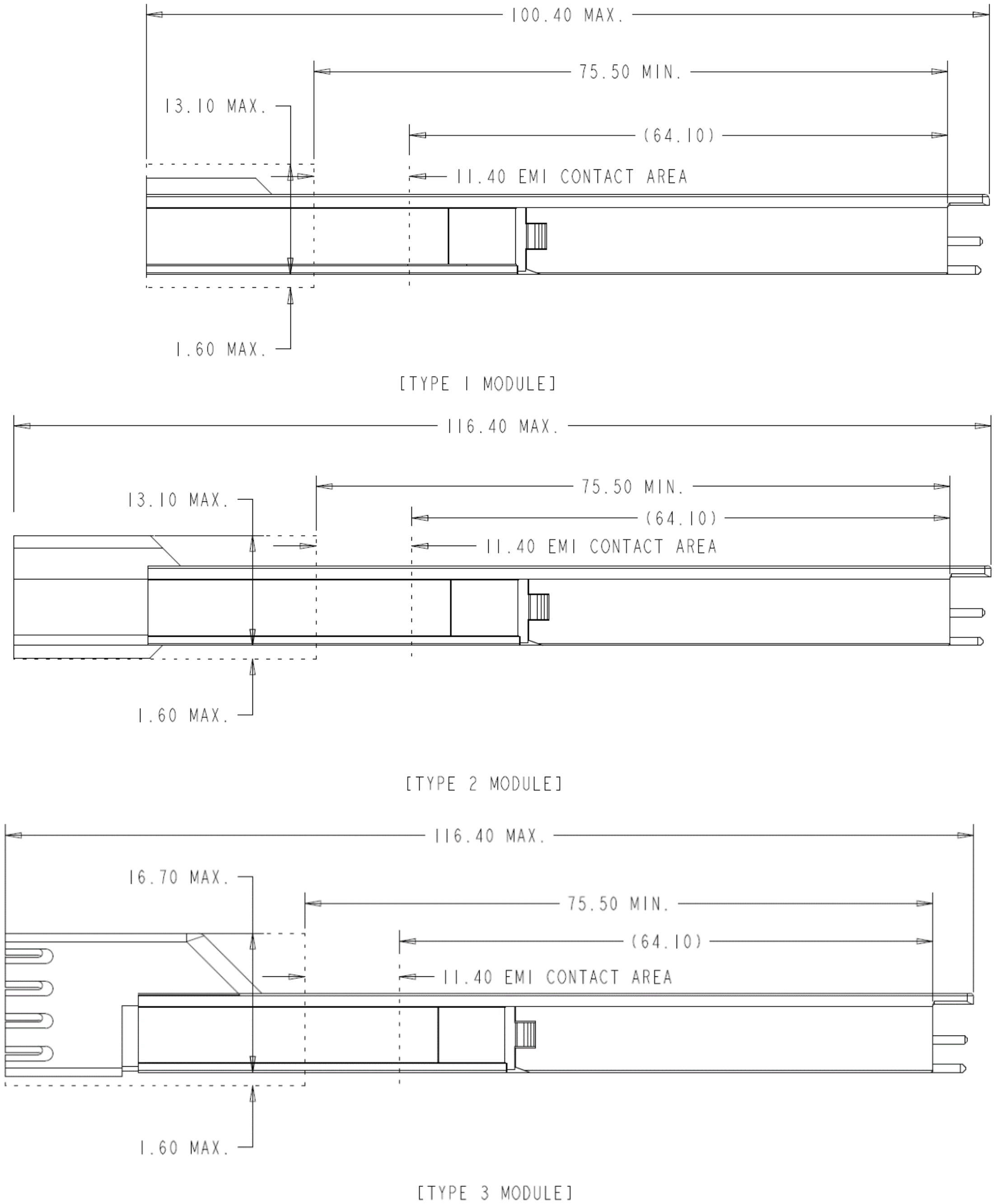


Figure 12-4: Size of OSFP-RHS module front, type 1, 2 and 3

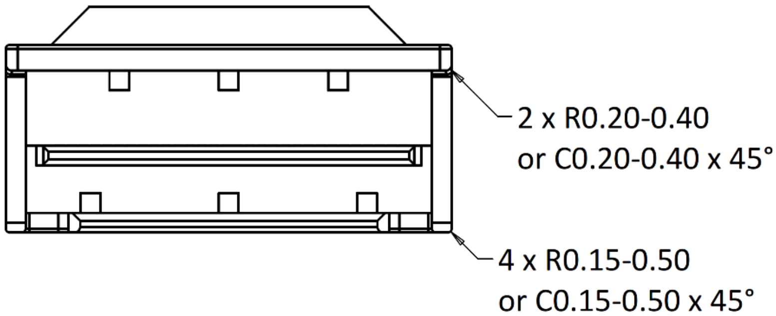


Figure 12-5: Corner radius of OSFP-RHS in back view

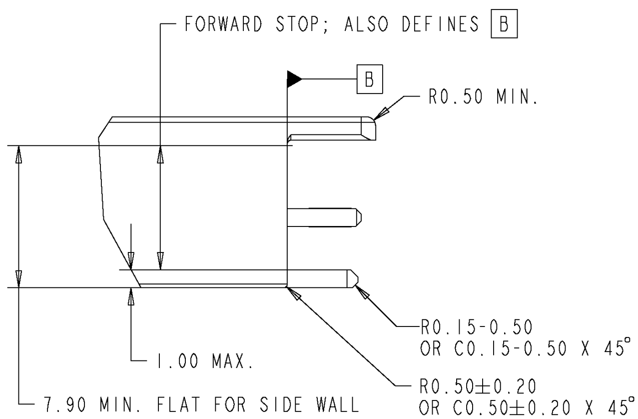


Figure 12-6: OSFP-RHS forward stop

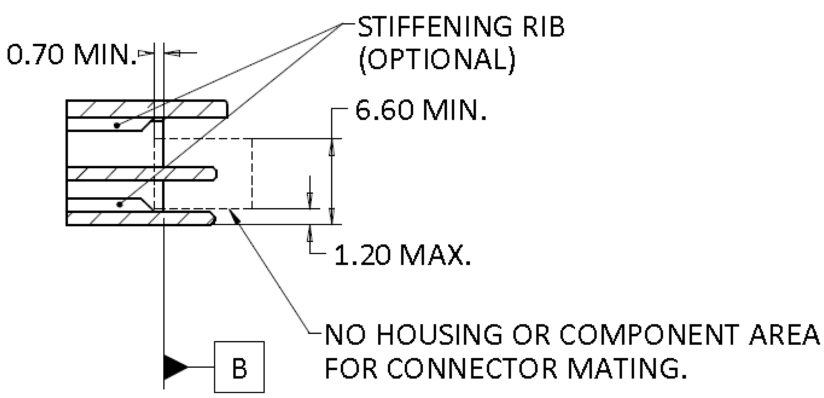


Figure 12-7: Connector keepout area (side view)

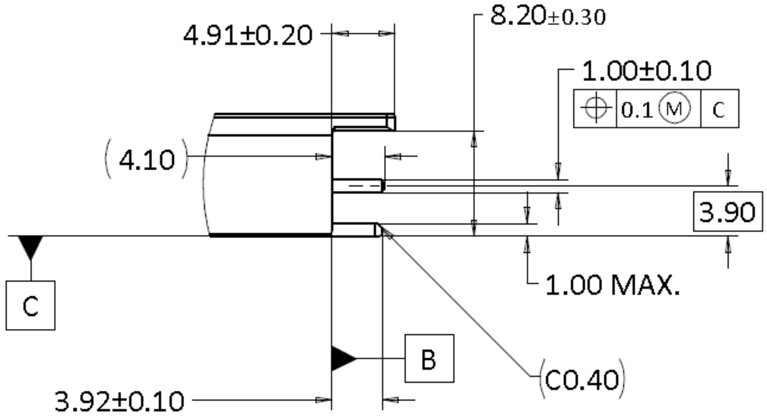


Figure 12-8: OSFP-RHS, back of the module

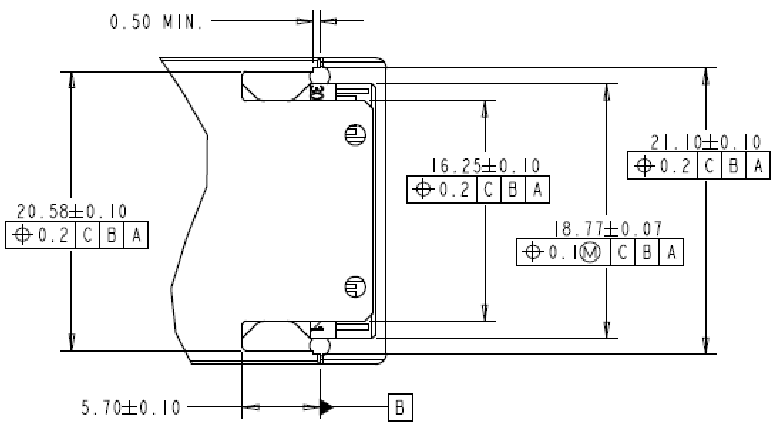


Figure 12-9: Paddle card position (bottom view of module)

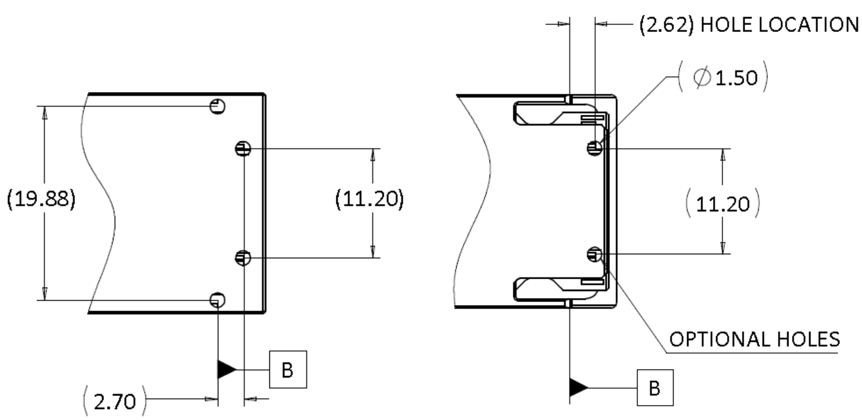


Figure 12-10: Location of inspection holes

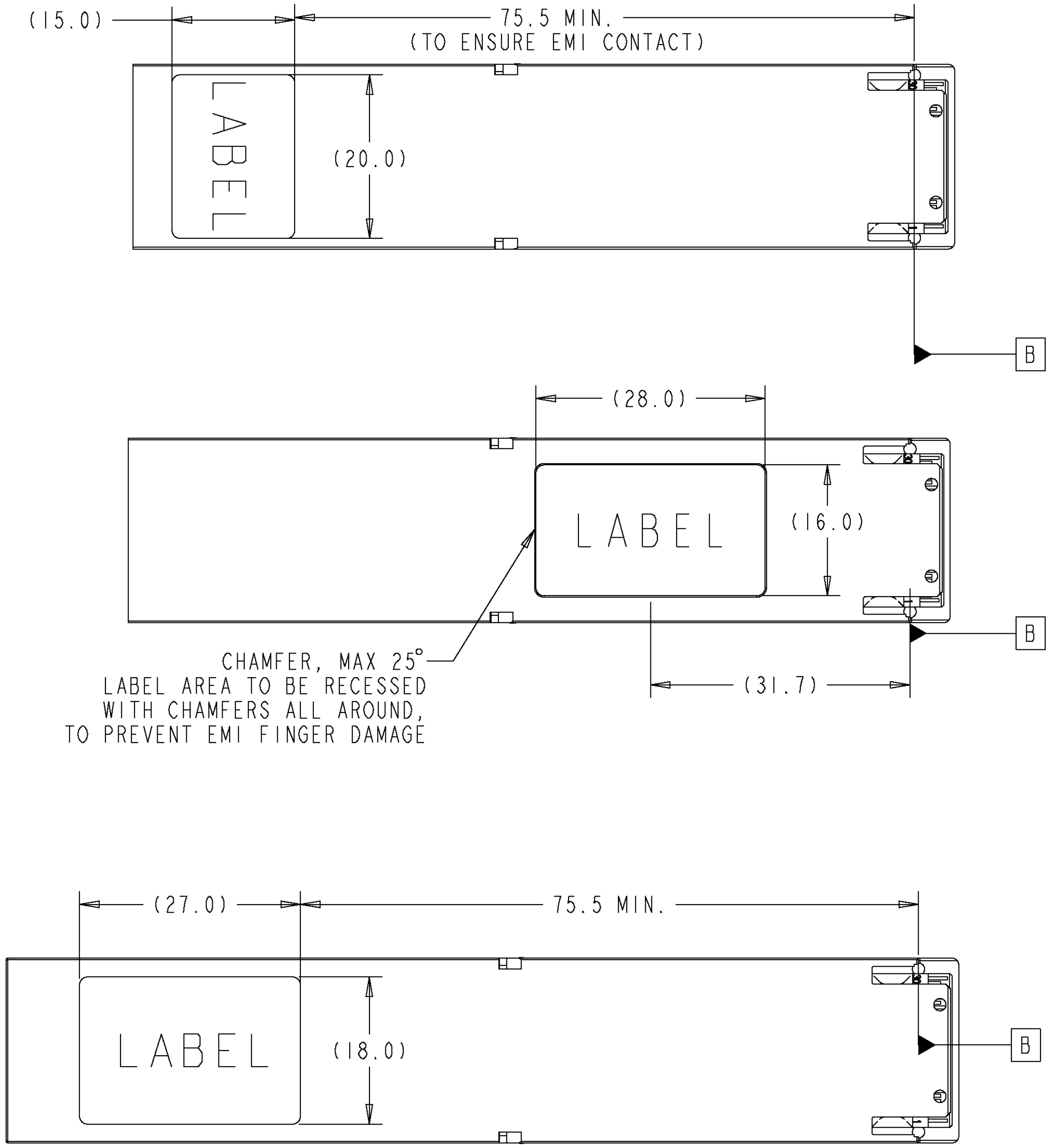


Figure 12-11: Label pocket for OSFP-RHS (Three reference locations)

12.3 OSFP-RHS, Card Edge and Latch Specification

This section applies only to the OSFP-RHS or OSFP800G-RHS. For the card edge design for the OSFP-RHS, refer Section 3.5, where the card edge design for the OSFP module is shown. Interface of the paddle card which mate with connector of an OSFP-RHS is identical with OSFP. Note that, as shown in the Figure 12-12, the shallow neck and the component place avoid area is optional in the OSFP-RHS.

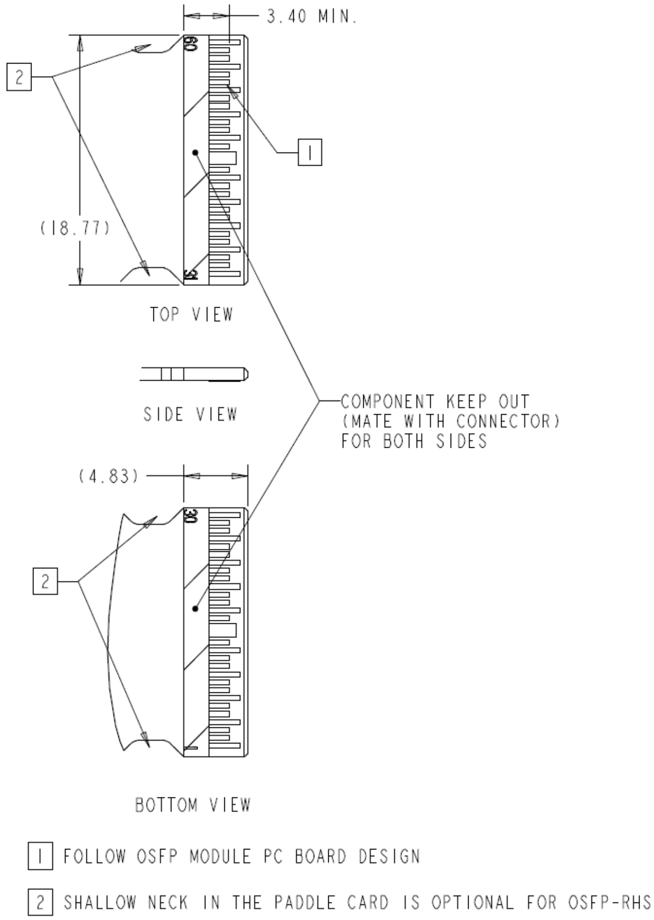


Figure 12-12: Paddle card of an OSFP-RHS

Figure 12-13 shows the location of the leading edge of the signal pad in the card edge, with respect to the module positive stop.

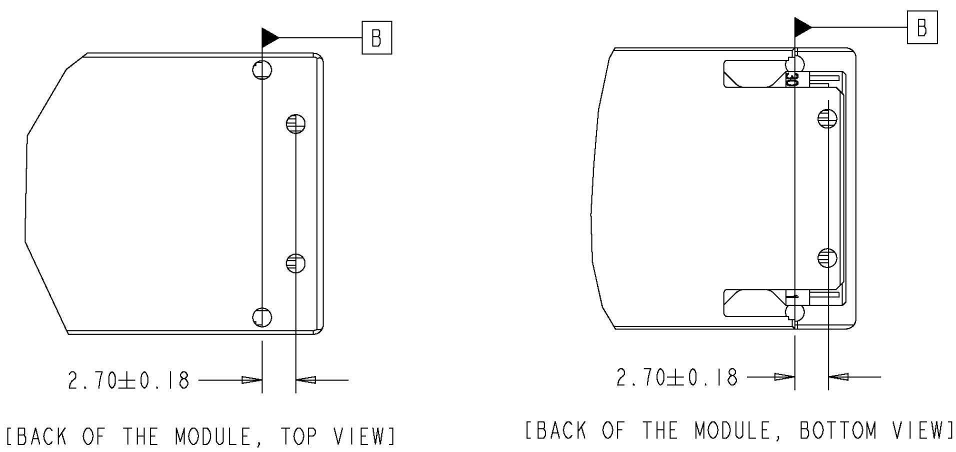


Figure 12-13: Leading edge of signal pad location, OSFP-RHS

The latching feature of the OSFP-RHS is based on the OSFP, but the location of the latching feature with respect to the module positive stop differs. Figure 12-14 shows the latch pocket detail of the OSFP-RHS. Also refer Figure 3-27, Figure 3-28 and Figure 3-29 for the further details of the latching features.

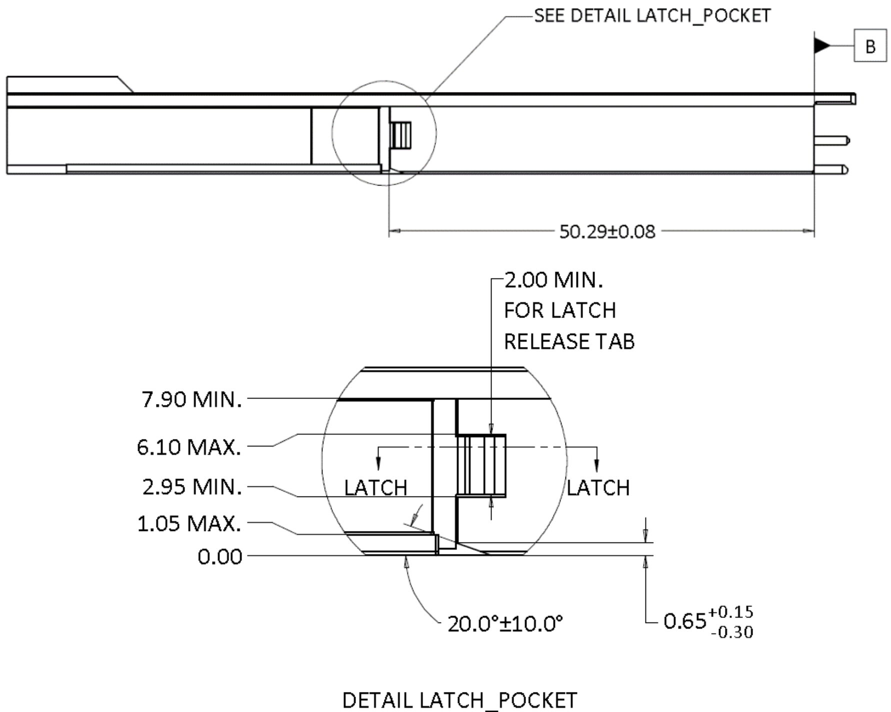


Figure 12-14: Latch pocket details of an OSFP-RHS (See section 3.7 for latch cross-section)

12.4 OSFP1600-RHS, Card Edge and Latch Specification

This section applies to OSFP1600-RHS. OSFP-RHS or OSFP800-RHS can either follow section 12.3 or this section; but the specification in the section should be applied as a whole, not partially applied or combined between the two sections.

As with OSFP1600, OSFP1600-RHS is expected to be used with OSFP1600-RHS compatible cage and connector, although the OSFP1600-RHS is still pluggable to the OSFP-RHS port and vice versa.

Figure 12-15 shows the location of the leading edge of the signal pad in the card edge, with respect to the module datum. Note that the location is slightly different when compared to the OSFP-RHS, with tighter tolerance.

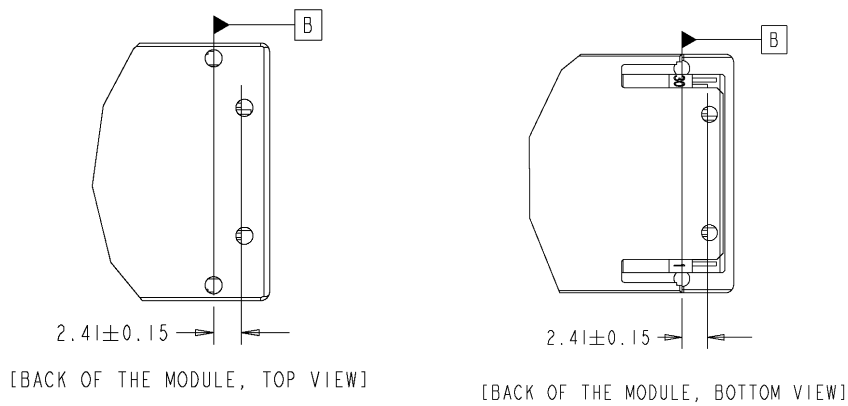


Figure 12-15: Leading edge of signal pad location, OSFP1600-RHS

For the card edge design for OSFP1600-RHS, refer to Section 4.2, where the card edge design for the OSFP1600 module is shown.

OSFP1600-RHS has a module latch feature that follows OSFP1600, as shown in the section 0. However, instead of Figure 4-7, Figure 12-16 should be applied, because the location of the latching feature to the module positive stop differs.

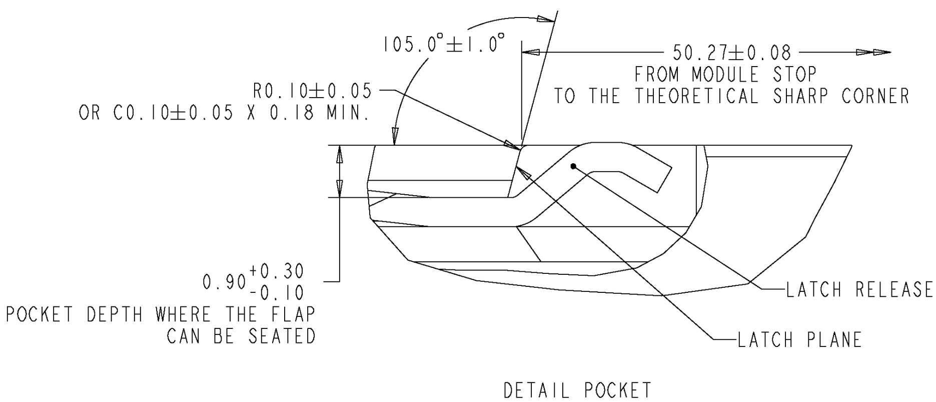


Figure 12-16: OSFP1600-RHS module latch pocket depth and angle

Rest of the specification in the section 4.3 is applied to OSFP1600-RHS.

12.5 OSFP-RHS Thermal Interface Surface Requirements

The thermally conductive area of an OSFP-RHS, as in the Figure 12-3, shall be compliant with specifications in Table 12-2.

Table 12-2: Surface flatness and roughness of the thermally conductive area

OSFP-RHS Power (Max)	Surface Flatness	Surface Roughness
Equal or less than 5W	0.15mm or better	Ra 3.2µm or better
More than 5W	0.075mm or better	Ra 1.6µm or better
More than 14W	0.05mm or better	Ra 0.8µm or better

12.6 OSFP-RHS Cage, Single Row, Mechanical Specification

An OSFP-RHS cage has a lower height than an OSFP cage and makes use of a riding heat sink for cooling. The forward stop feature in an OSFP-RHS cage is shifted compared with an OSFP cage to match an OSFP-RHS module. See Figure 12-17 to Figure 12-24 for the mechanical specification of the cage for OSFP-RHS. The host PCB footprint is identical to OSFP. Its latch feature is identical, except its geometrical reference (forward stop) has been moved.

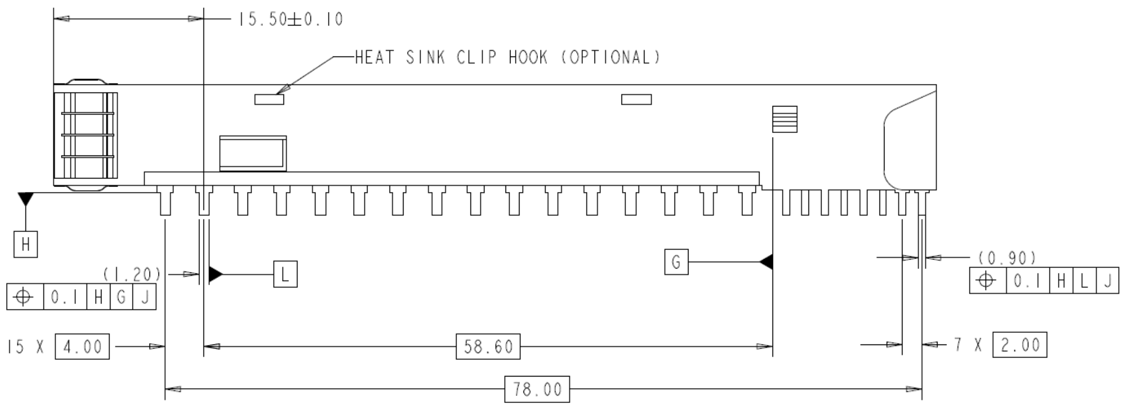


Figure 12-17: Cage positioning pins and forward stop

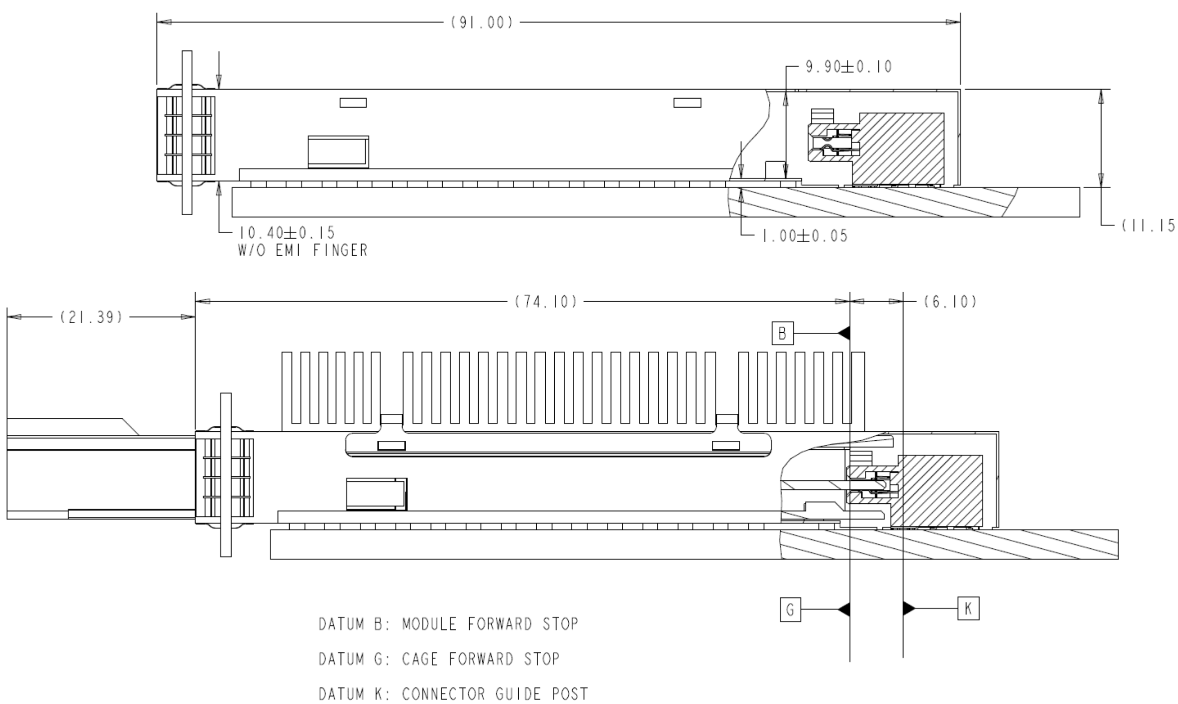


Figure 12-18: Side view of a 1x1 cage with vertical cage dimensions

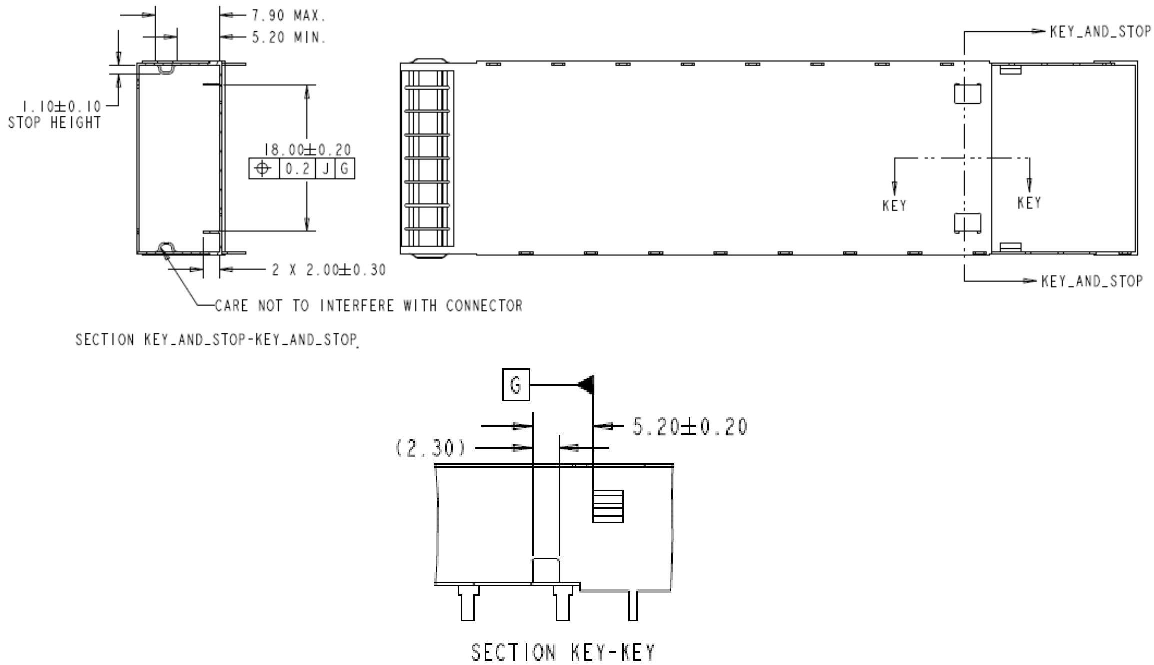


Figure 12-19: Keying feature in OSFP-RHS

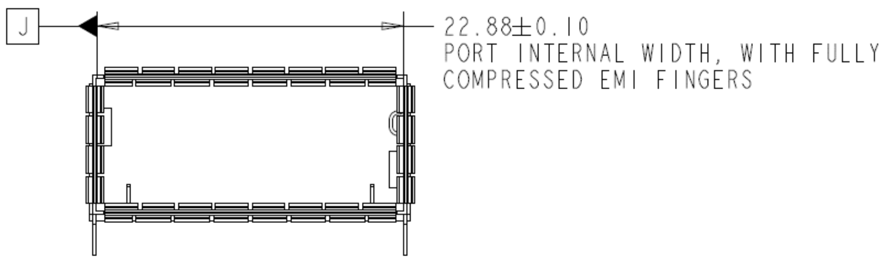
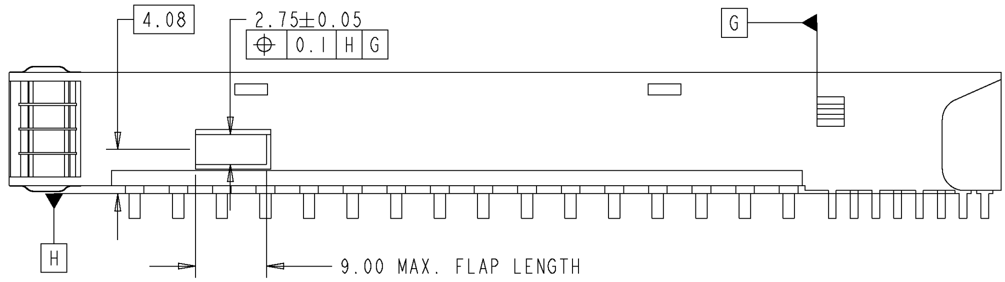
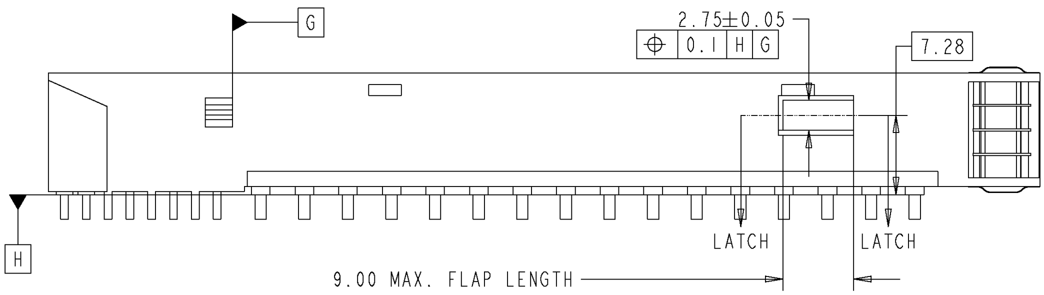


Figure 12-20: Internal width and centerline datum





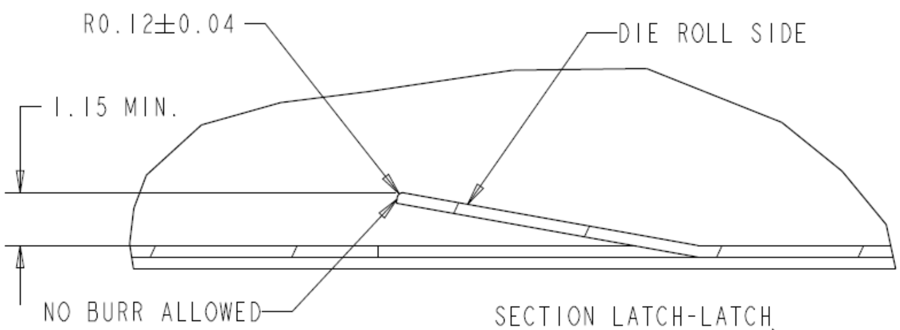


Figure 12-21: Latch feature for OSFP-RHS cage

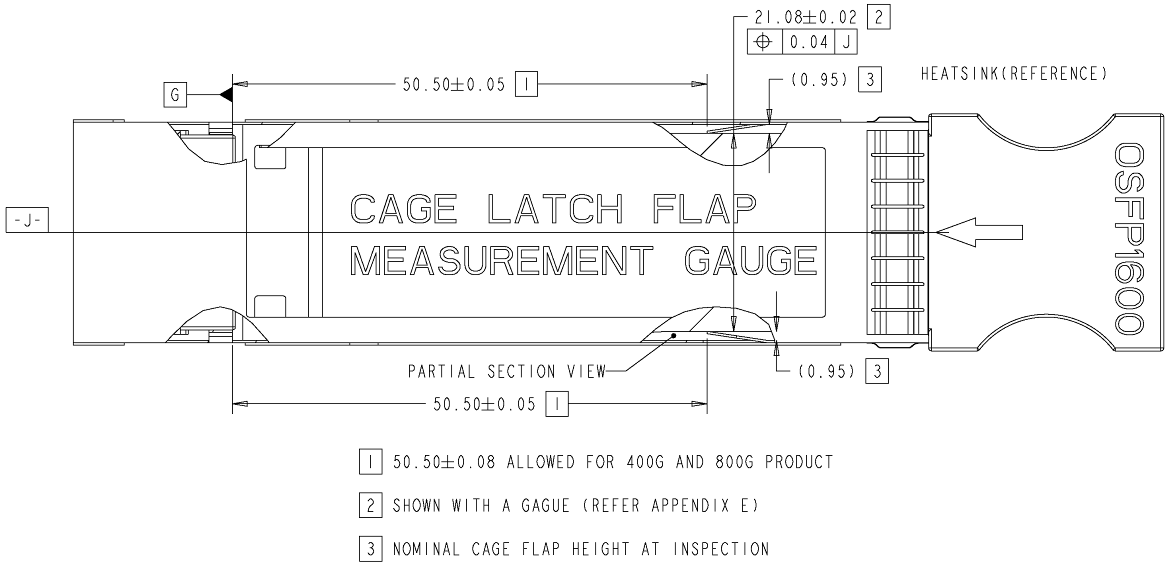


Figure 12-22: Latch location for OSFP-RHS cage

Note that for the cage to be used with OSFP-RHS and OSFP800-RHS only, a larger tolerance in the latch location is allowed, as shown in the Figure 12-22.

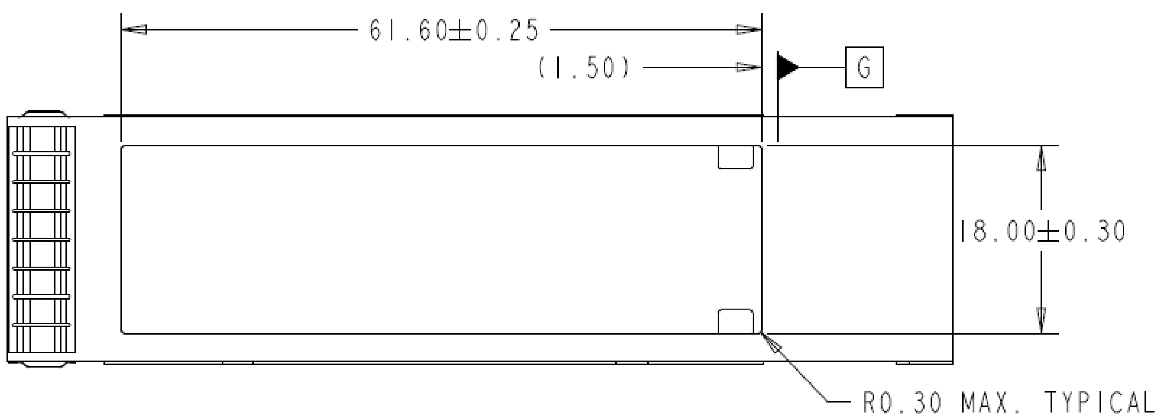


Figure 12-23: Cutout for a riding heat sink in the OSFP-RHS cage

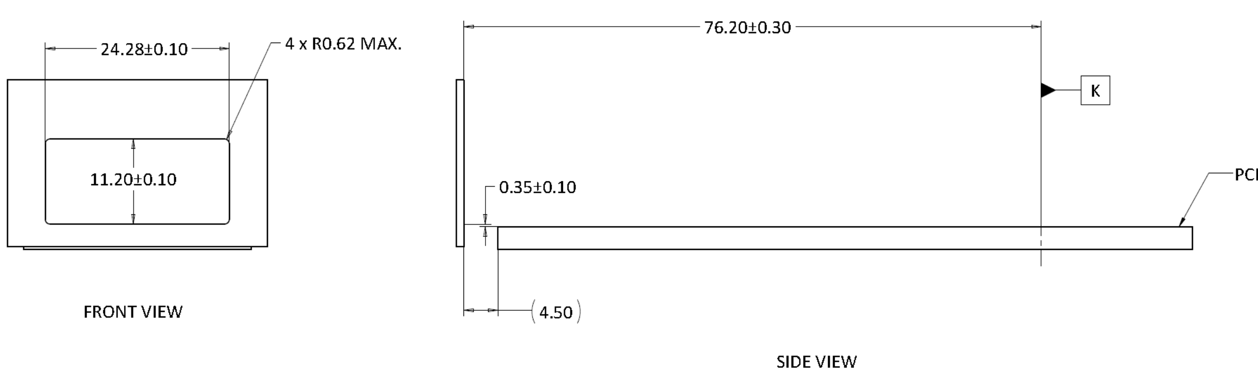


Figure 12-24: Bezel cutout for the OSFP-RHS cage

12.7 OSFP-RHS Cage, Stacked, Mechanical Specification

In this section, a stacked cage for OSFP-RHS is shown. This cage is to be used with OSFP stacked connector with 19.9mm pitch, as in the section 7.3.2.

Figure 12-25 shows the overview of the stacked cage with an OSFP-RHS module. The shape and the size of the heatsink may vary, and perforation of the cage may also vary per application.

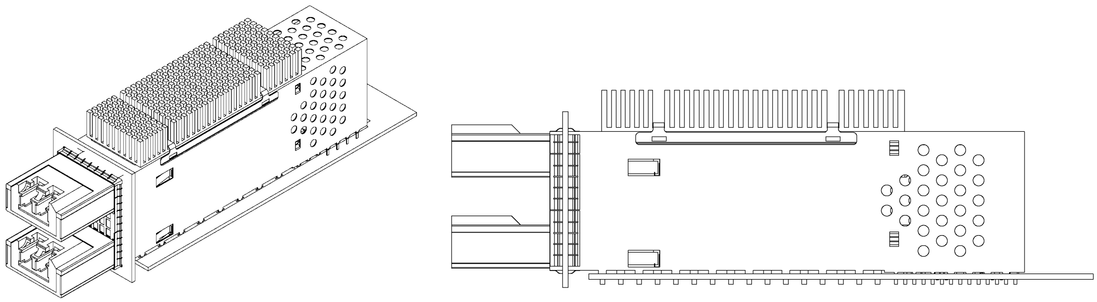


Figure 12-25: Stacked OSFP-RHS cage (Left: ISO view, Right: side view)

Figure 12-26 shows the length and height of the cage.

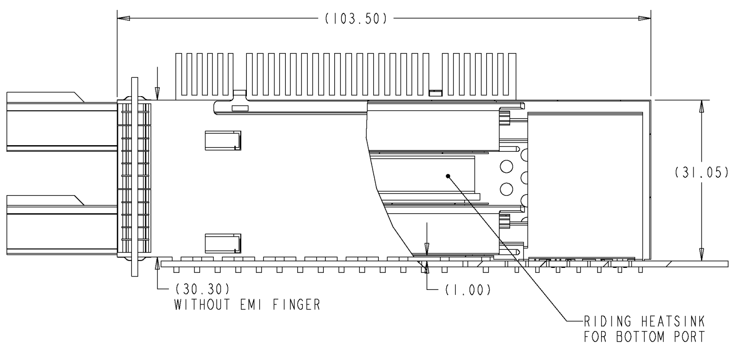


Figure 12-26: Side partial section view of stacked OSFP-RHS (With host board, connector, cage, module, riding heatsink and panel)

Figure 12-27 shows that the cage have 19.9mm pitch between the top and the bottom port, while the port size is designed to match with OSFP-RHS.

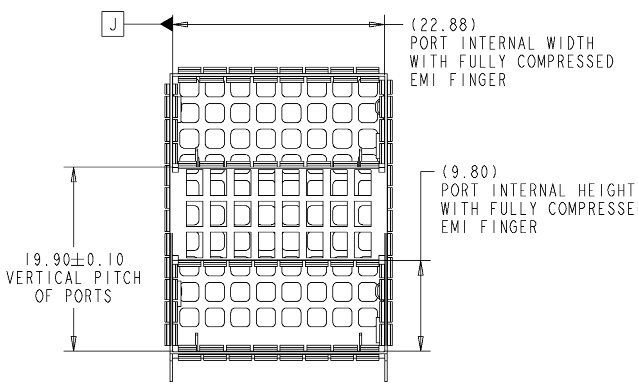


Figure 12-27: Port internal width and height of stacked OSFP-RHS

This cage is designed to have same footprint with OSFP stacked SMT cage and connector, as in the section 7.4 to 7.6. Figure 12-28 shows the compliance pin location for the cage.

Considering the cage forward stop is shifted 5.7mm from OSFP cage, the compliance pins are in the same nominal location with OSFP stacked SMT cages.

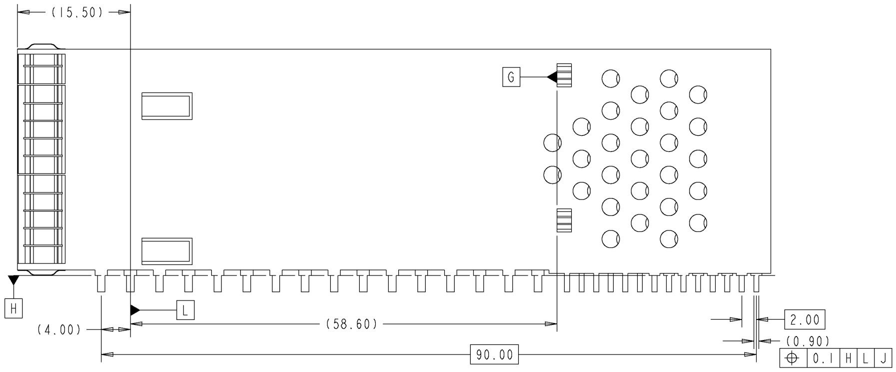


Figure 12-28: Compliance pin location, stacked OSFP-RHS

Figure 12-29 shows the heatsink cutout for the top port and the bottom port. Note that the riding heatsink cutout for the bottom port is smaller than the top port, to avoid the interference with the connector during the assembly. The size of the riding heatsink cutout for the top port is matching with single row OSFP-RHS as in the Figure 12-23, while for the bottom port it is matching with OSFP as in the Figure 5-13.

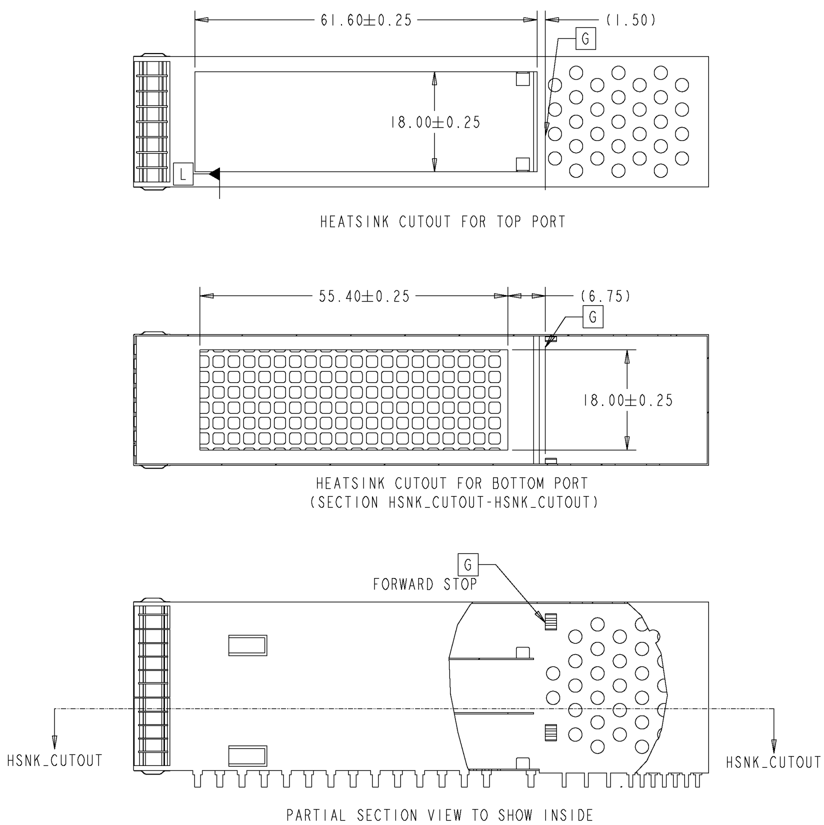


Figure 12-29: Cutout for a riding heat sink in the stacked OSFP-RHS cage

Figure 12-30 shows the nominal clearance between the cage and the connector, which shows that there is no interference between the connector and cage in this reference dimension.

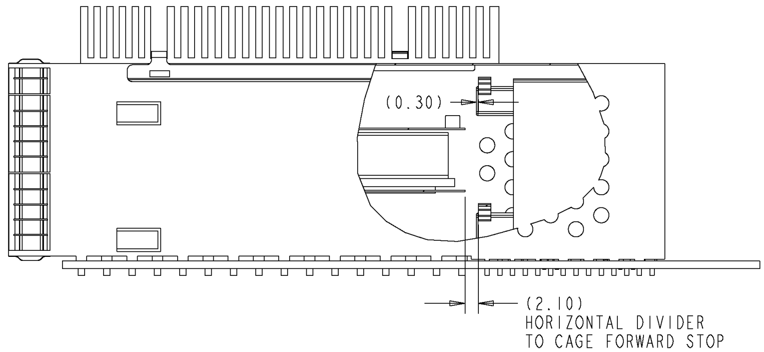


Figure 12-30: Horizontal divider to cage stop and connector (reference dimension)

Figure 12-31 shows the panel size for the stacked OSFP-RHS cage to make EMI contact with the cage and the panel.

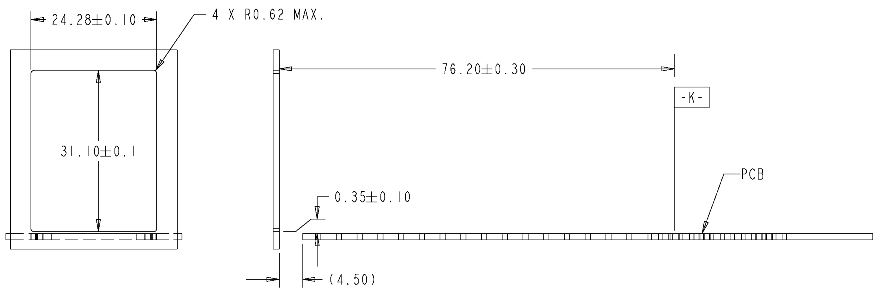


Figure 12-31: Panel size for stacked OSFP-RHS cage

Figure 12-32 shows the location of the latching flap, which complies with OSFP 19.9mm stacked cage as shown in the Figure 7-25.

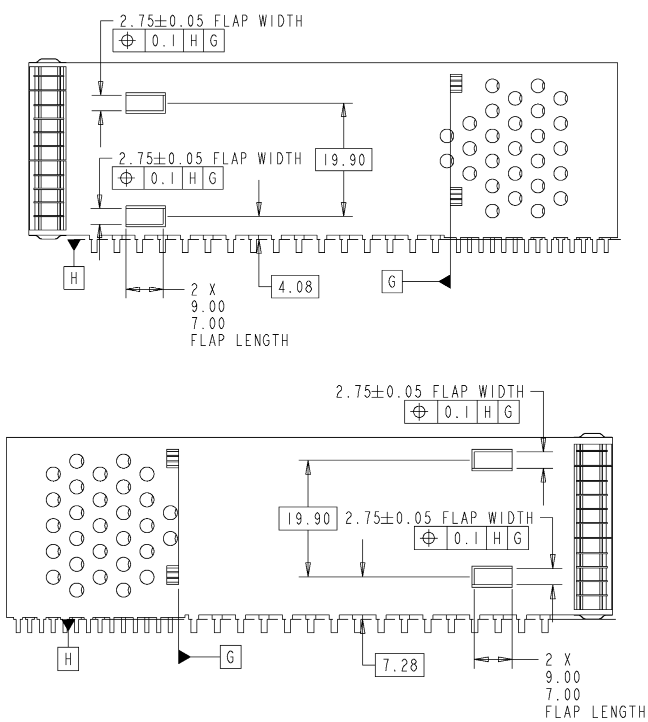


Figure 12-32: Latching flap location and size for stacked OSFP-RHS

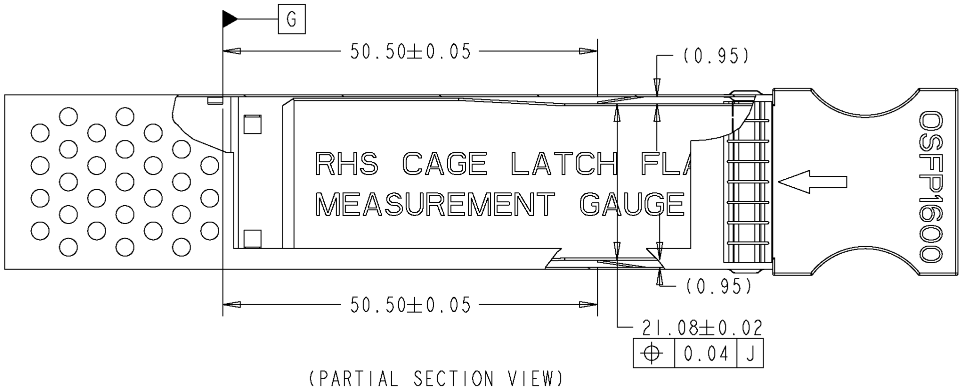


Figure 12-33: Location of latching flap with respect to the forward stop

Figure 12-33 shows the location of the latching flap.

12.8 Maximum Heat Sink Down Force for an OSFP-RHS Cage

The cage should be designed so that the down force which will be applied from the riding heat sink to an OSFP-RHS module should not exceed 50N.

12.9 Custom Height OSFP-RHS

There may be a custom OSFP-RHS with height different than 9.5mm but otherwise having all other attributes of OSFP-RHS. Details of such custom height OSFP-RHS are not provided in this specification.

13 Optical PMD Block Diagrams

Below sub-sections illustrate block diagrams for a sampling of optical physical medium dependent sublayers (PMDs) that can be realized in an OSFP form factor. These block diagrams are meant to serve as guidelines for better understanding of the form factor and are by no means exhaustive.

13.1 400G PDM Block Diagrams

13.1.1 Optical PMD for parallel single mode fiber: 400G-DR4 / 400G-DR4-2

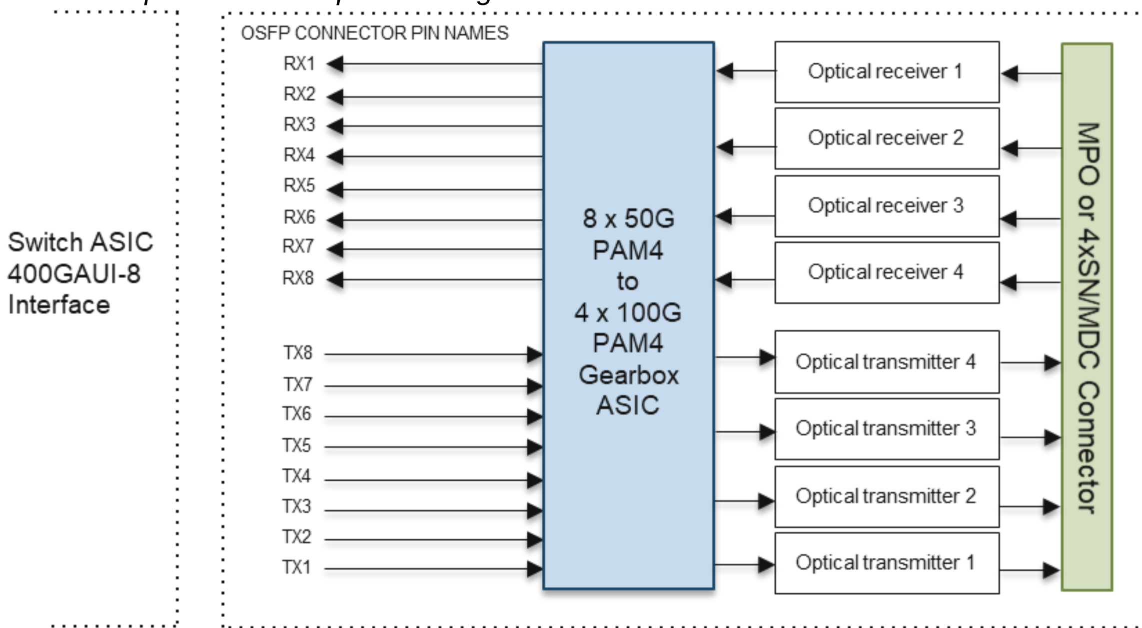


Figure 13-1: Block diagram, 400G-DR4 / 400G-DR4-2

13.1.2 Optical PMD for parallel multi mode fiber: 400G-SR8

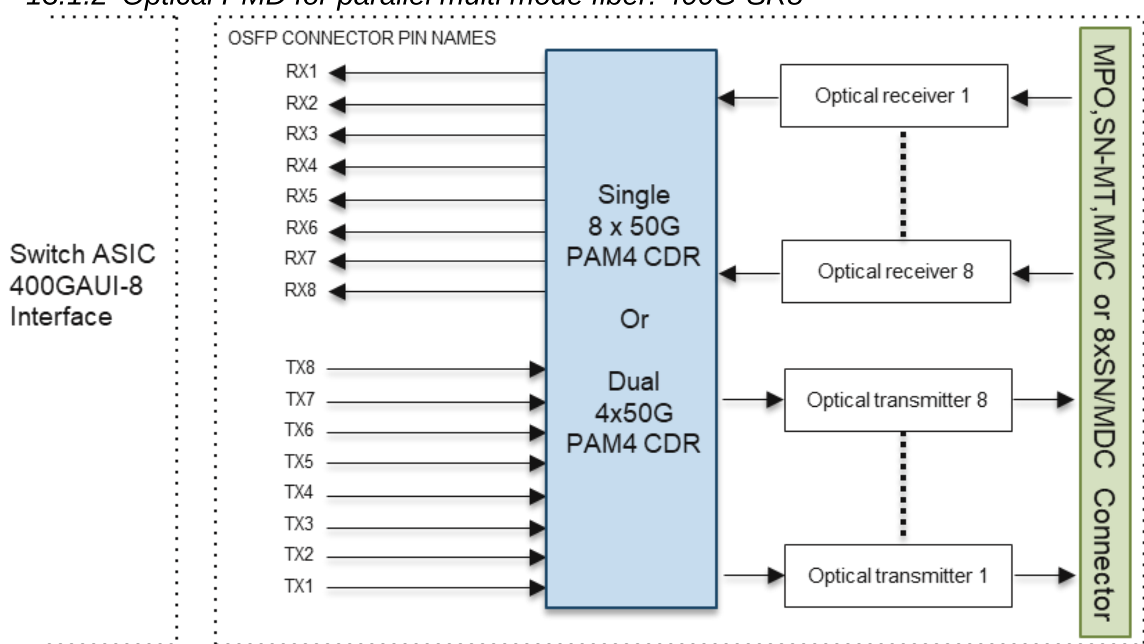


Figure 13-2: Block diagram, 400G-SR8

13.1.3 Optical PMD for parallel multi mode fiber: 400G-SR4.2

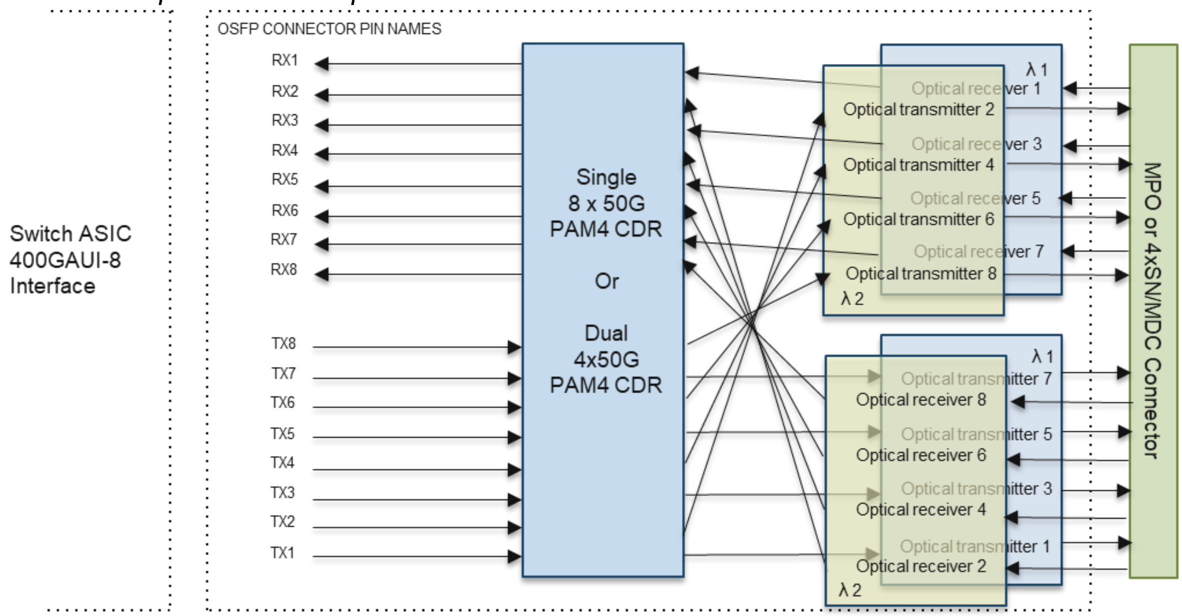


Figure 13-3: Block diagram, 400G-SR4.2

13.1.4 Optical PMD for duplex single mode fiber: 400G-FR4 / 400G-FR4-500

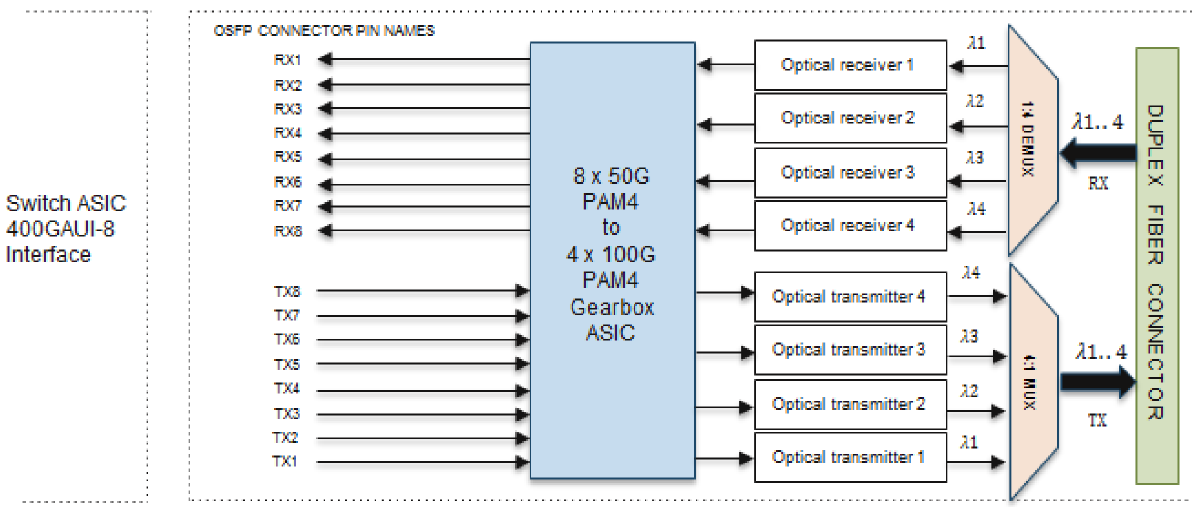


Figure 13-4: Block diagram, 400G- FR4 / 400G-FR4-500

13.1.5 Optical PMD for duplex single mode fiber: 400G-FR8/LR8

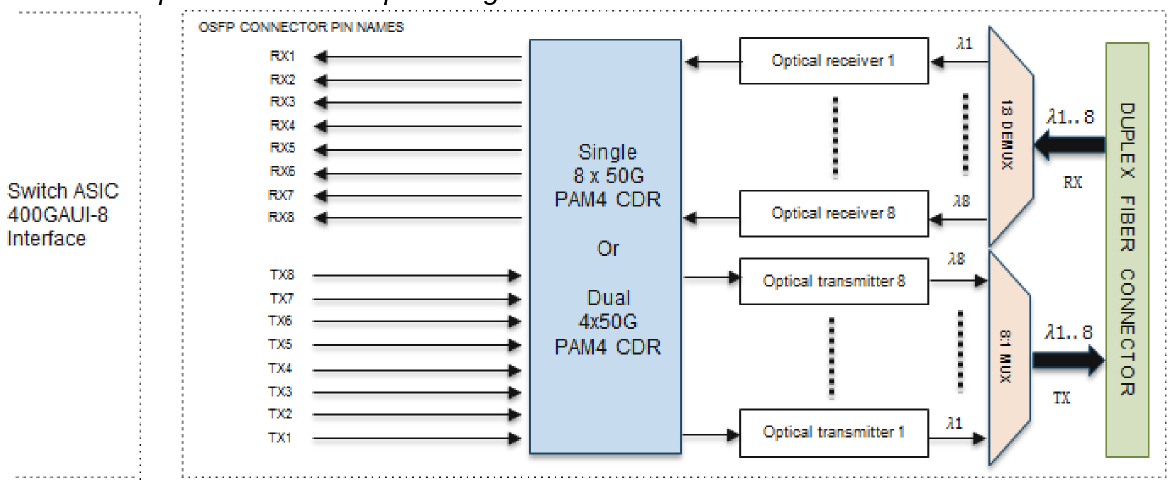


Figure 13-5: Block diagram, 400G-FR8/LR8

13.1.6 Optical PMD for dual duplex single mode fiber: 2x200G-FR4 / 2X200G-FR4-500

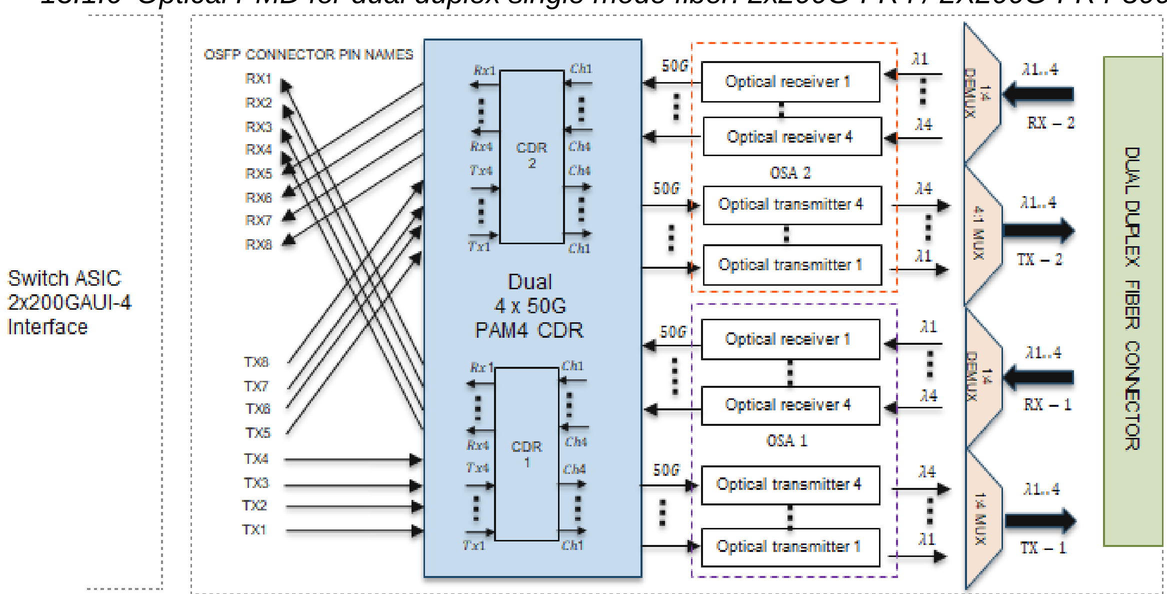


Figure 13-6: Block diagram, 2x200G- FR4 / 2X200G-FR4-500

13.1.7 Optical PMD for dual duplex single mode fiber: 2x100G-2xCWDM4

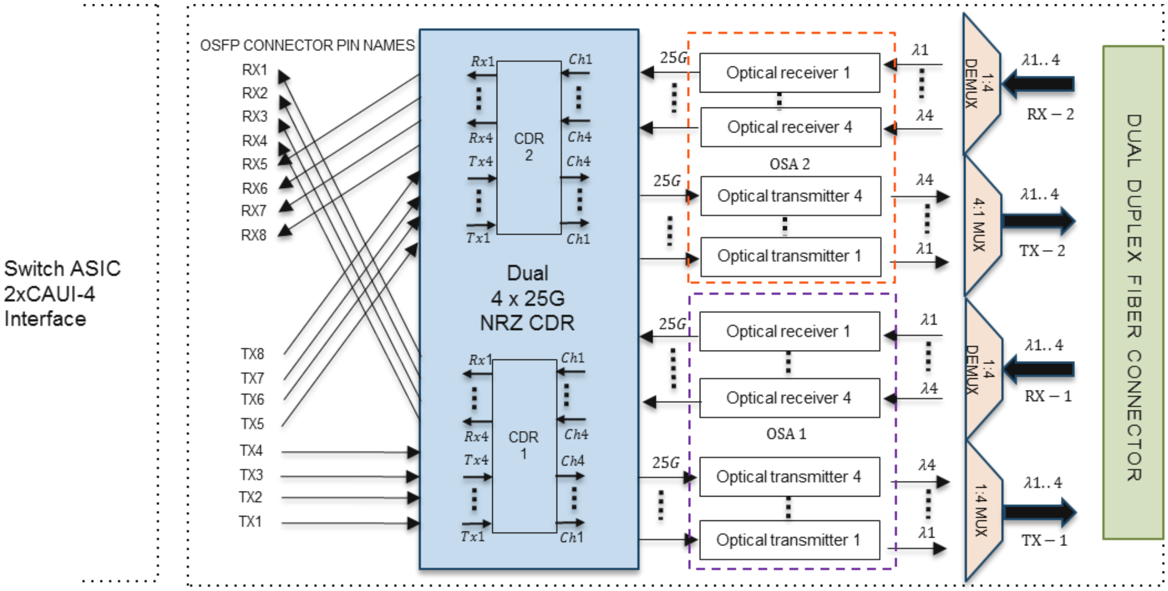


Figure 13-7: Block diagram, 2×100G-2xCWDM4

13.2 800G PMD Block Diagrams

13.2.1 Optical PMD for 1λ SMF solution: 800G DR8 / 800G DR8-2

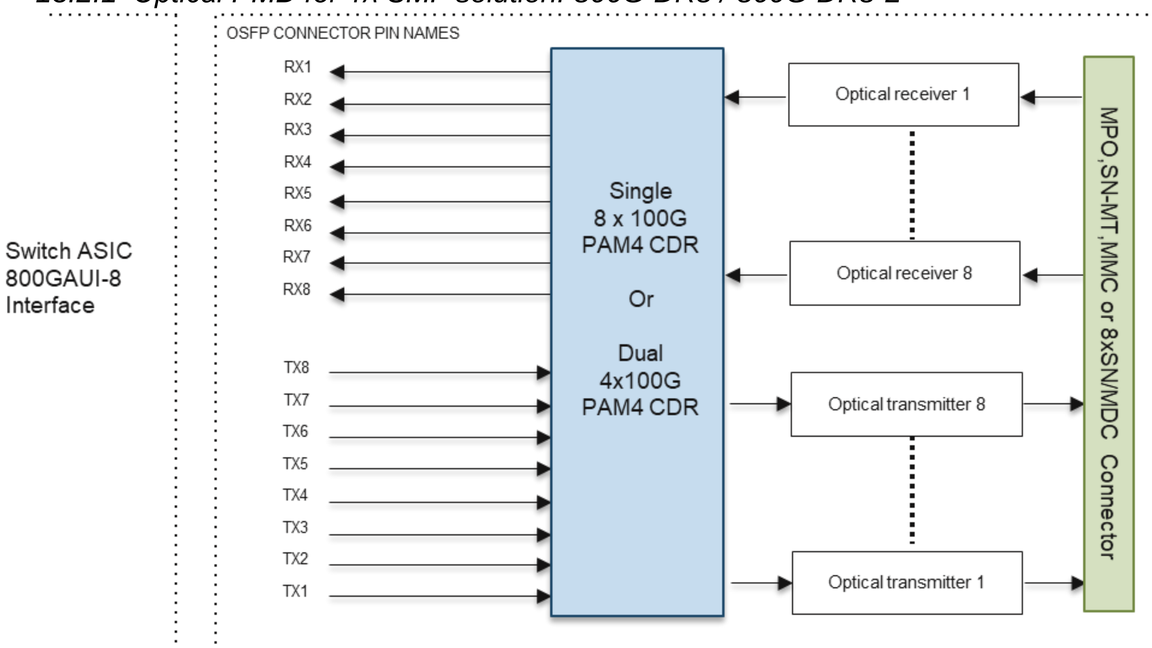


Figure 13-8: Block diagram, OSFP800 optical PMD for parallel fiber, e.g., 800G DR8 / 800G DR8-2

13.2.2 Optical PMD for 2λ SMF/MMF solution: 800G-VR/SR4.2 & 800G-DR4.2

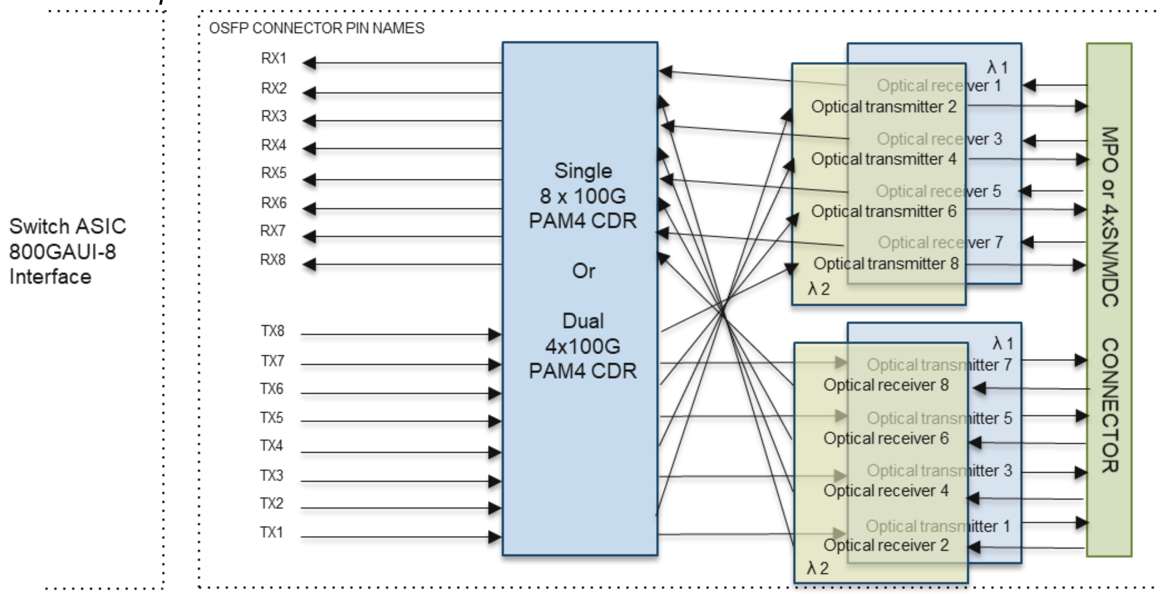


Figure 13-9: Block diagram, 800G- VR/SR4.2 & 800G-DR4.2

13.2.3 Optical PMD for 4λ SMF solution: 2xFR4 / 2xFR4-500

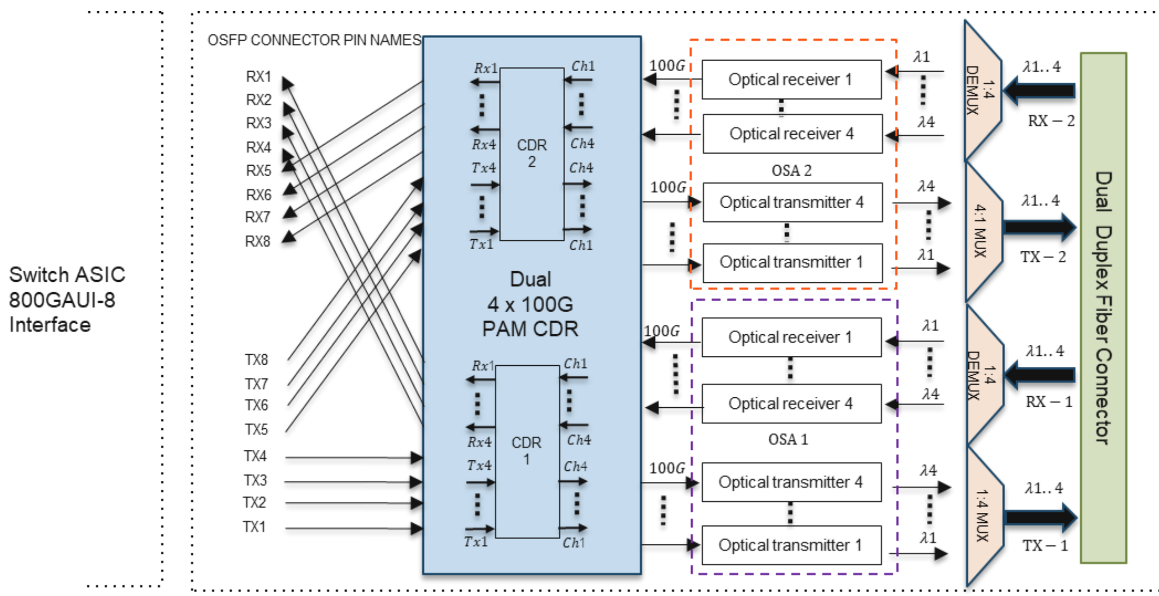


Figure 13-10: Block diagram, e.g. 2x400G FR4 / 2x400G FR4-500

13.2.4 Optical PMD for 4λ SMF solution: FR4 / FR4-500

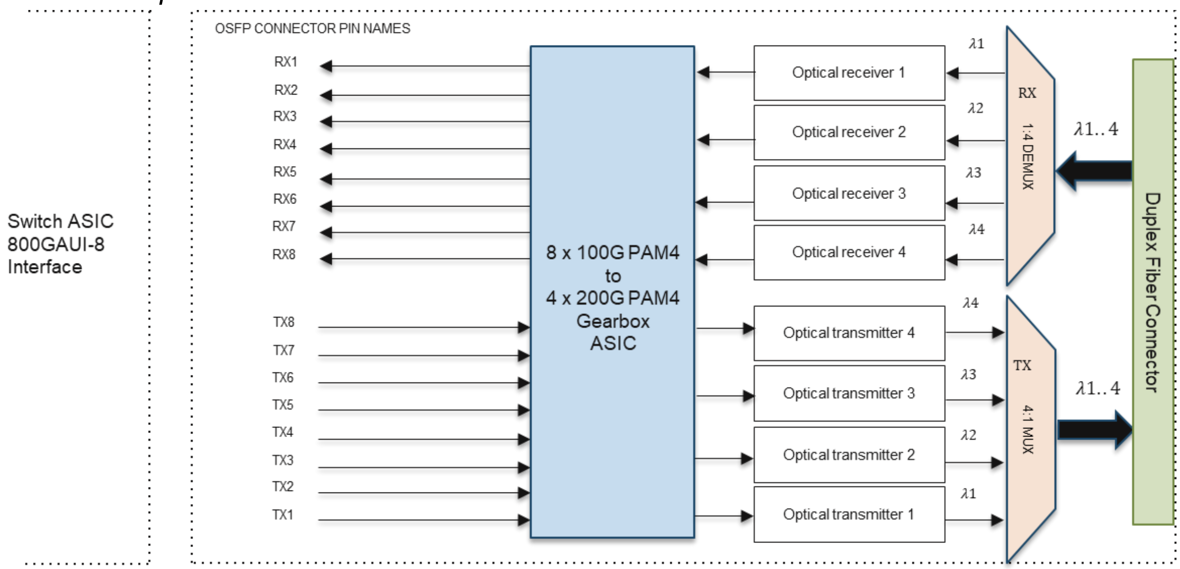


Figure 13-11: Block diagram, OSFP800 optical PMD for duplex fiber, e.g., 800G FR4 / 800G FR4-500

13.2.5 Optical PMD for 8λ SMF solution: FR8/LR8

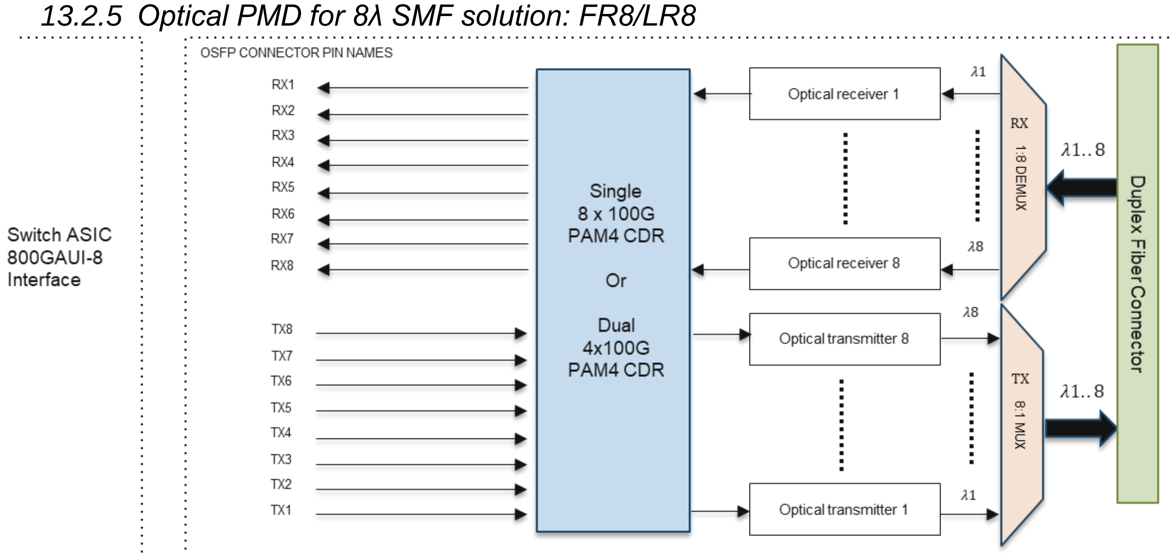


Figure 13-12: Block diagram, OSFP800 optical PMD for duplex fiber, e.g., 800G, FR8/LR8

13.2.6 Optical PMD for 1λ MMF solution: 800G SR8

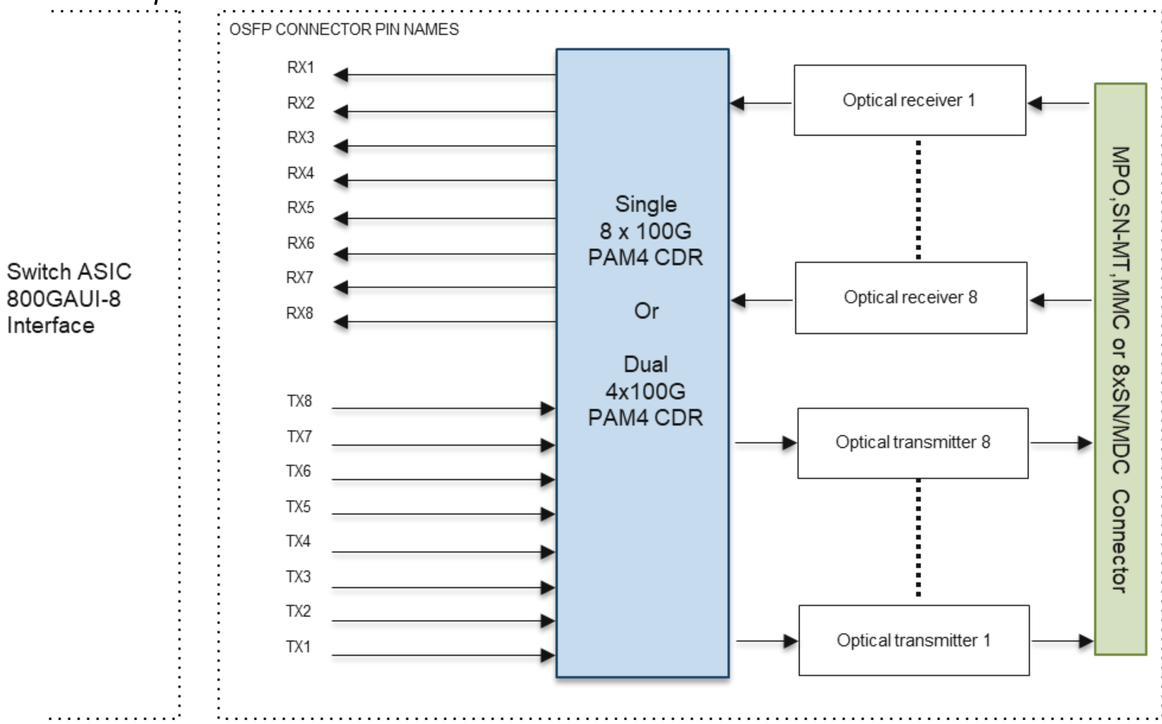


Figure 13-13: Block diagram, OSFP800 optical PMD for parallel fiber, e.g., 800G SR8

13.2.7 Optical PMD for 4λ MMF solution: 2x400G VR/SR SWDM4

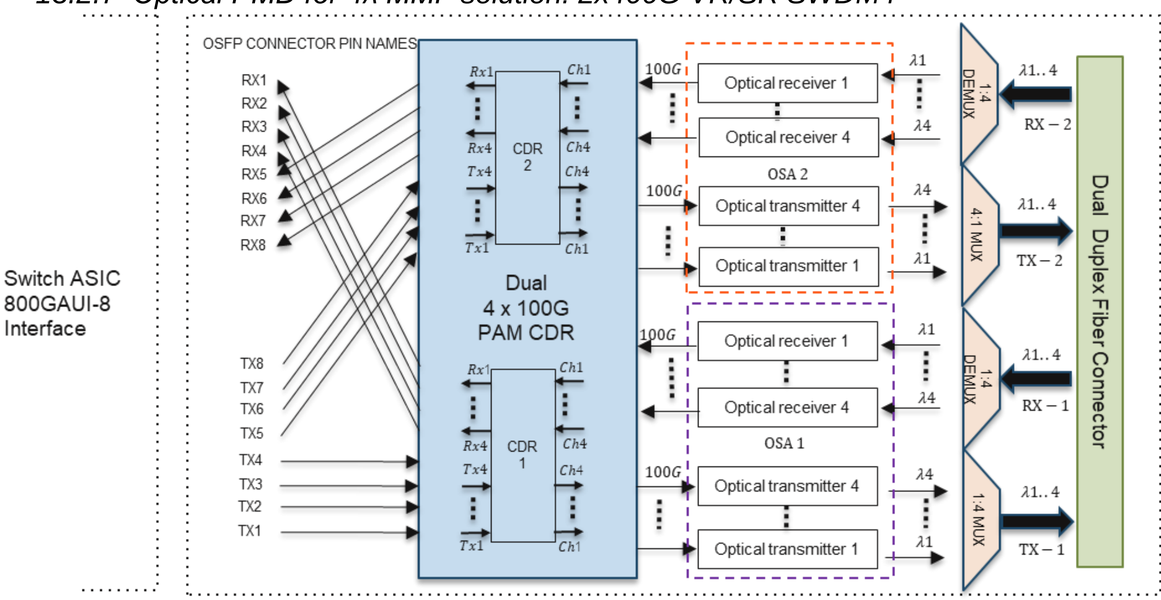


Figure 13-14: Block diagram, 2x400G VR/SR SWDM4

13.3 1600G PMD Block Diagrams

13.3.1 Optical PMD for 1λ SMF Solution-1: 1600G DR8 / 1600G DR8-2

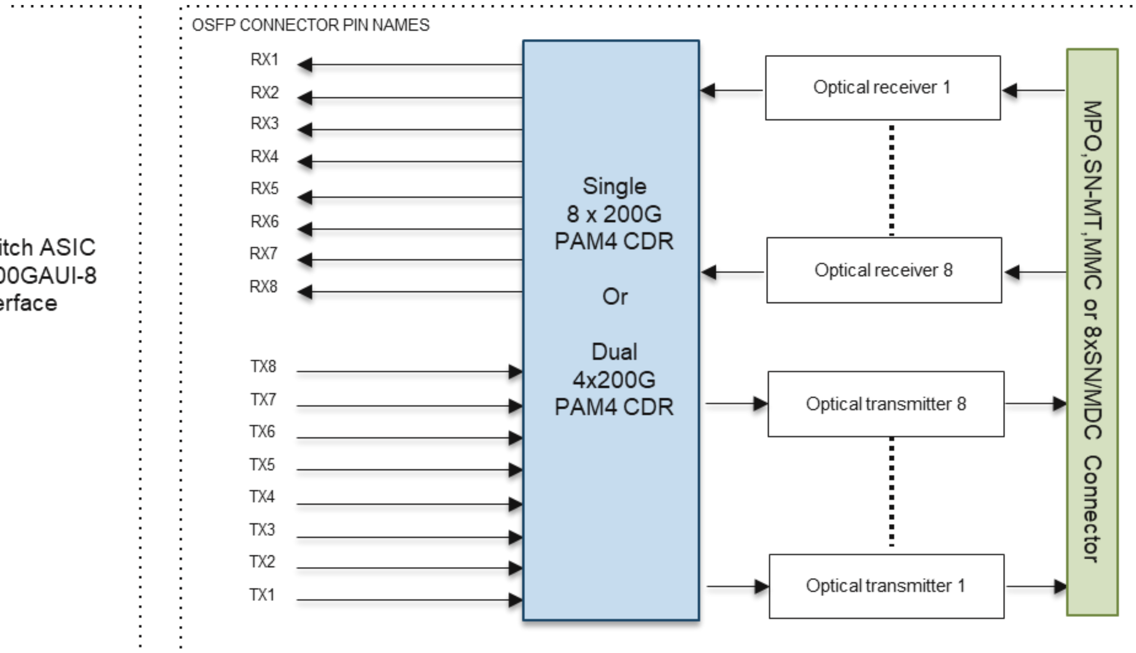


Figure 13-15: Block diagram, OSFP1600 optical PMD for parallel fiber, e.g., 1600G DR8 / 1600G DR8-2

13.3.2 Optical PMD for 1λ SMF Solution-2: 1600G Coherent

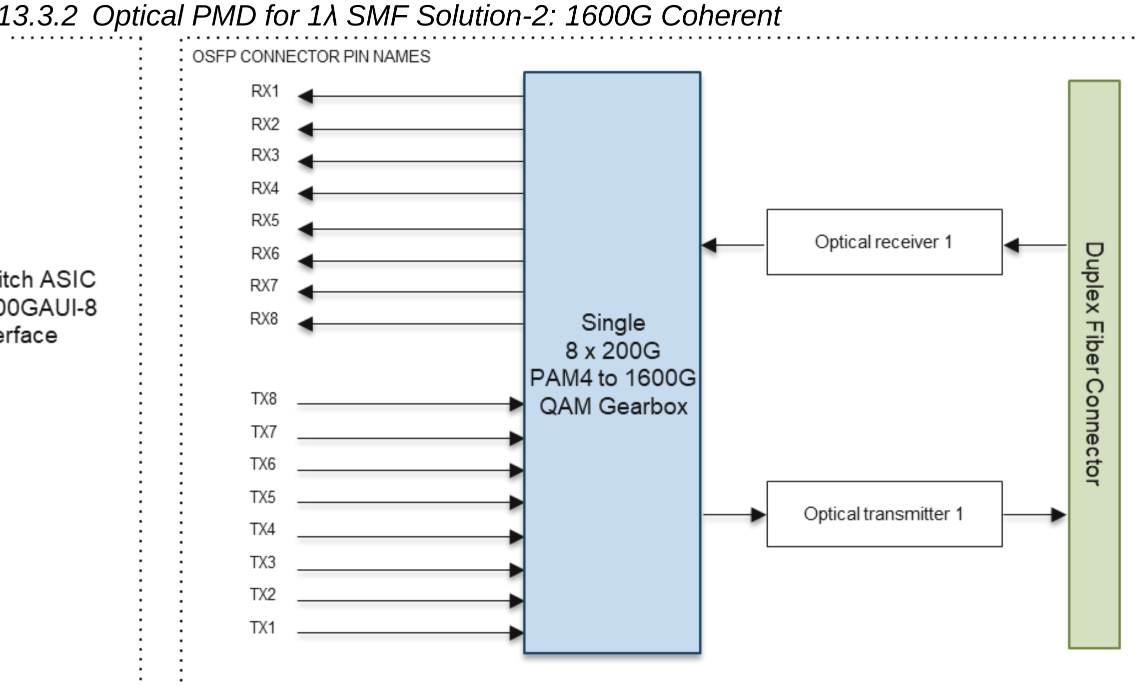


Figure 13-16: Block diagram, OSFP1600 optical PMD for duplex fiber, e.g., 1600G coherent

13.3.3 Optical PMD for 1λ SMF Solution-3: 2x800G Coherent

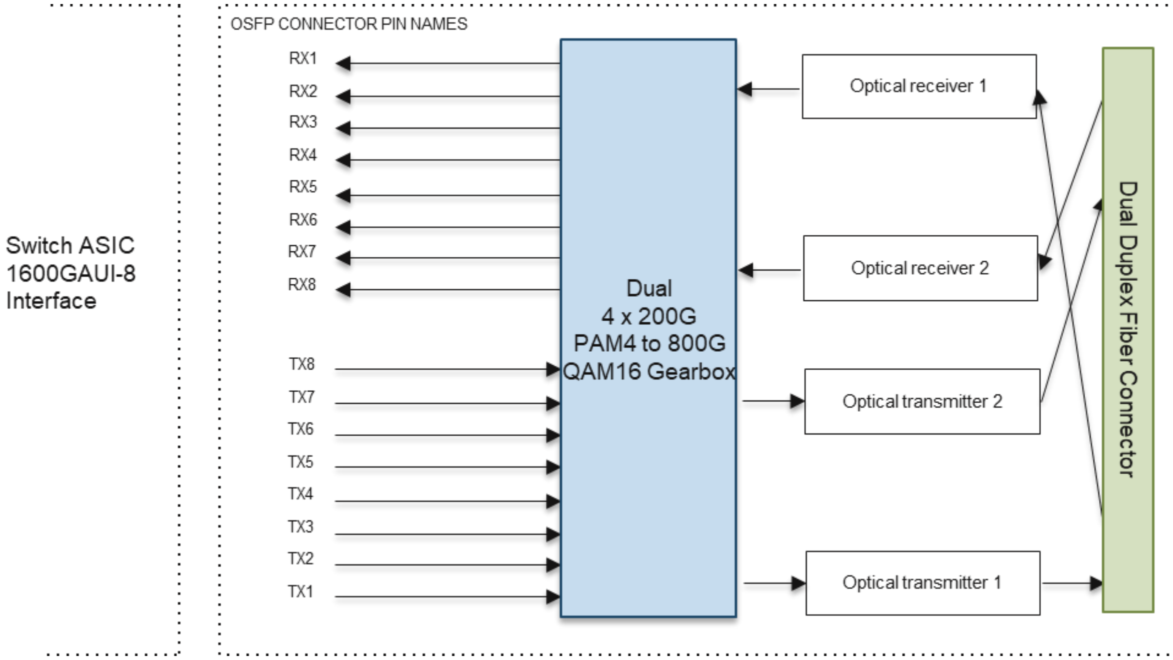


Figure 13-17: Block diagram, OSFP1600 optical PMD for dual duplex fiber, e.g., 2x800G coherent

13.3.4 Optical PMD for 1λ SMF Solution-4: 4x400G Coherent

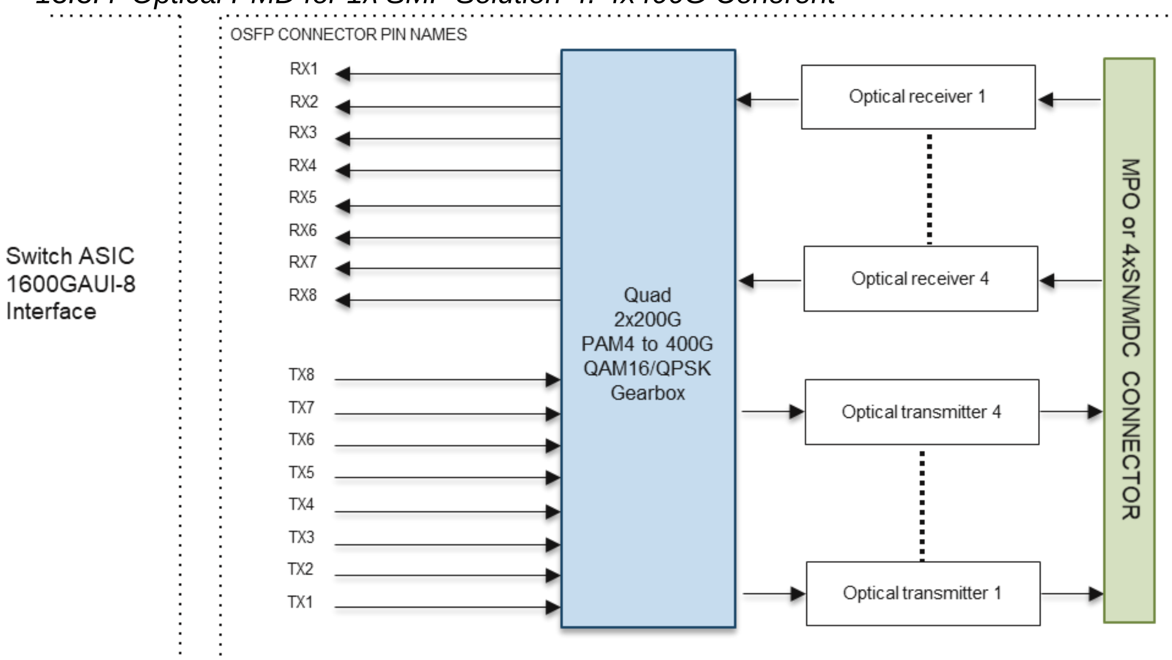


Figure 13-18: Block diagram, OSFP1600 optical PMD for parallel fiber, e.g., 4x400G coherent

13.3.5 Optical PMD for 2λ SMF Solution: 1600G-DR4.2

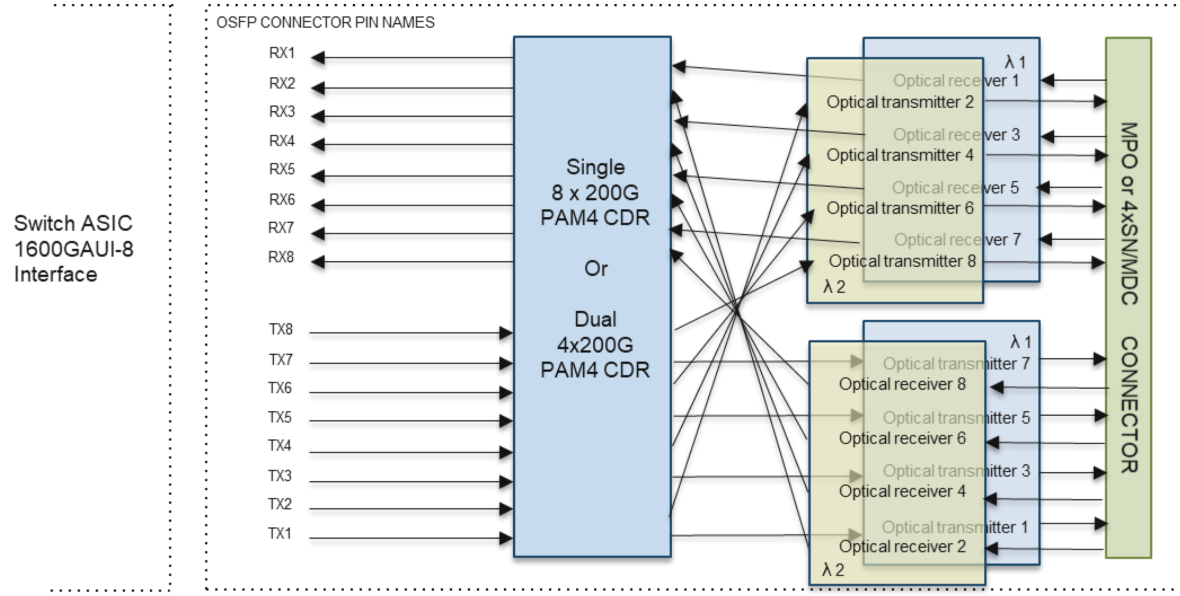


Figure 13-19: Block diagram, OSFP1600 optical PMD for 1600G-DR4.2

13.3.6 Optical PMD for 4λ SMF Solution-1: 2xFR4 / 2xFR4-500

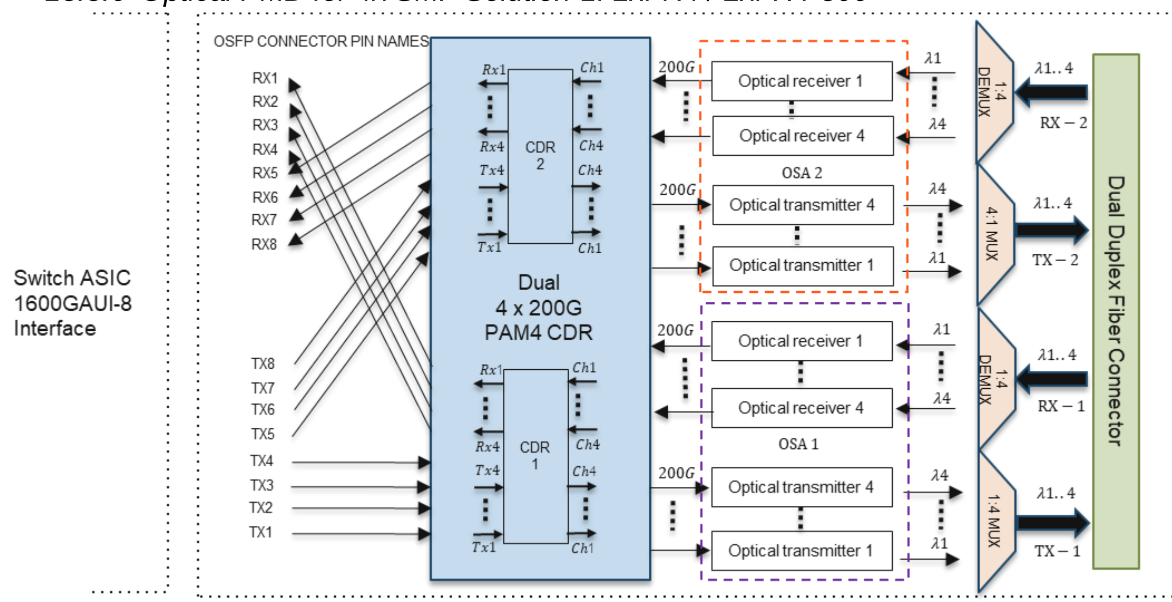


Figure 13-20: Block diagram, OSFP1600 optical PMD for 2x800G FR4 / 2x800G FR4-500

13.3.7 Optical PMD for 4λ SMF Solution-2: FR4 / FR4-500

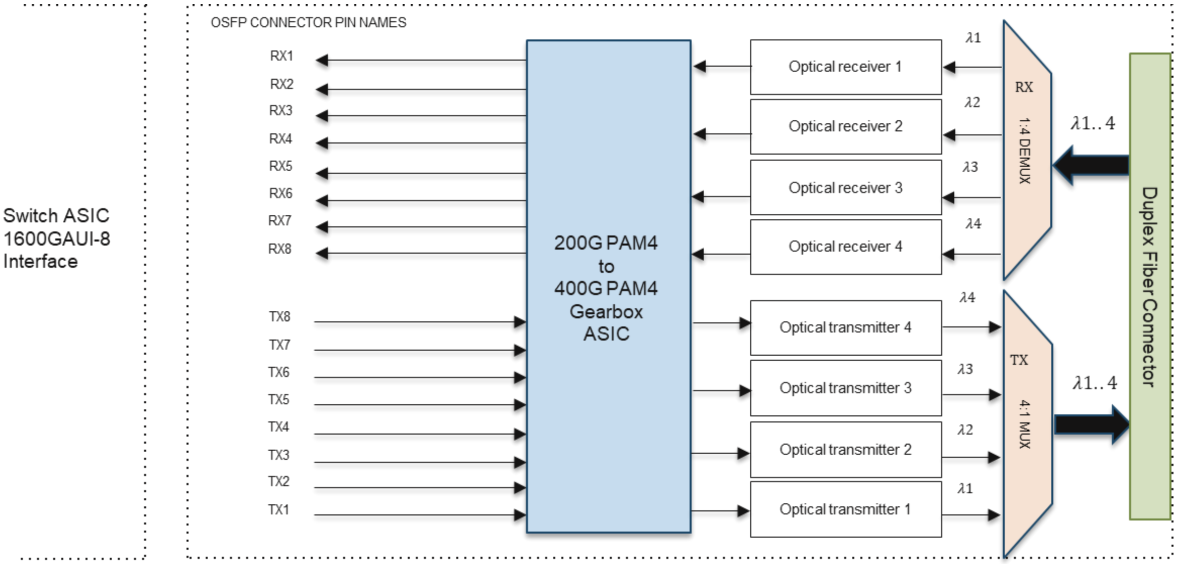


Figure 13-21: Block diagram, OSFP1600 optical PMD for duplex fiber, e.g., 1600G FR4 / 1600G FR4-500

13.3.8 Optical PMD for 4λ SMF Solution-3: 4x400G ZR4

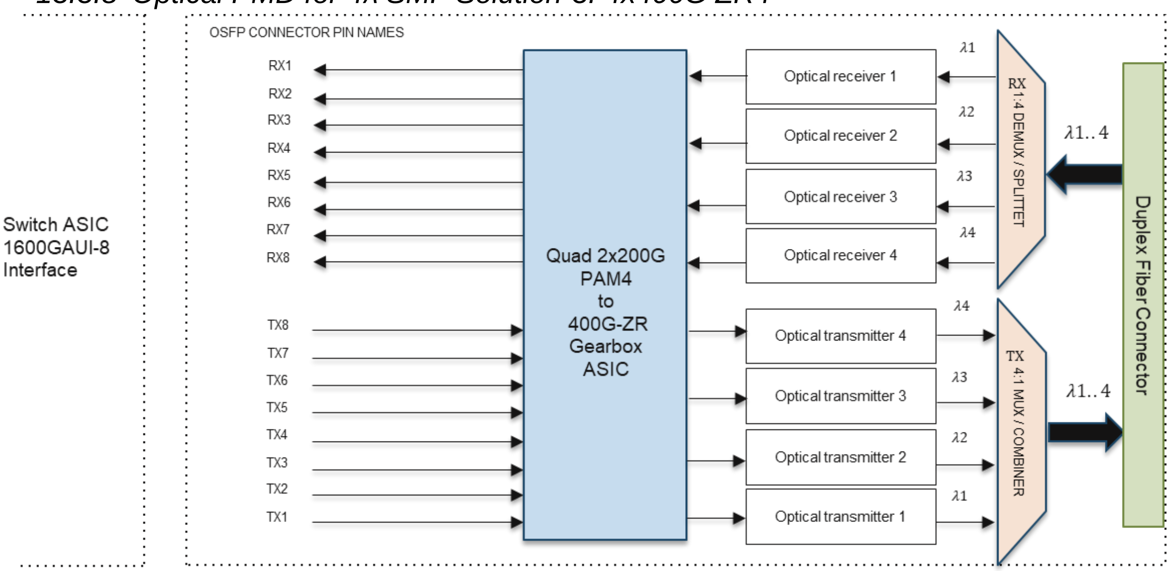


Figure 13-22: Block diagram, OSFP1600 optical PMD for duplex fiber, e.g., 4x400G ZR4

13.3.9 Optical PMD for 8λ SMF Solution: FR8/LR8

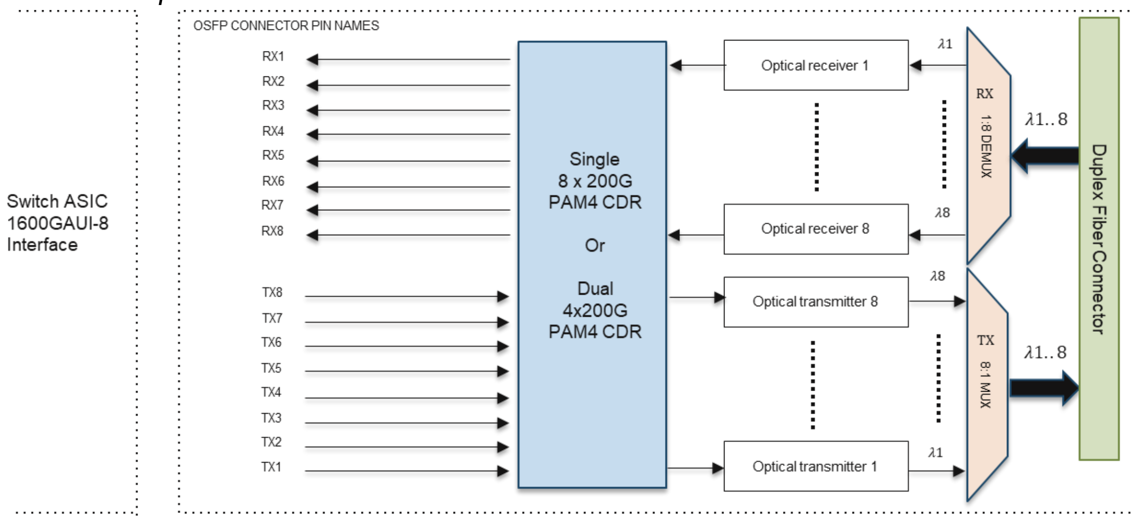


Figure 13-23: Block diagram, OSFP1600 optical PMD for 1600G FR4/LR8

13.3.10 Optical PMD for 1λ MMF Solution: 1600G SR16

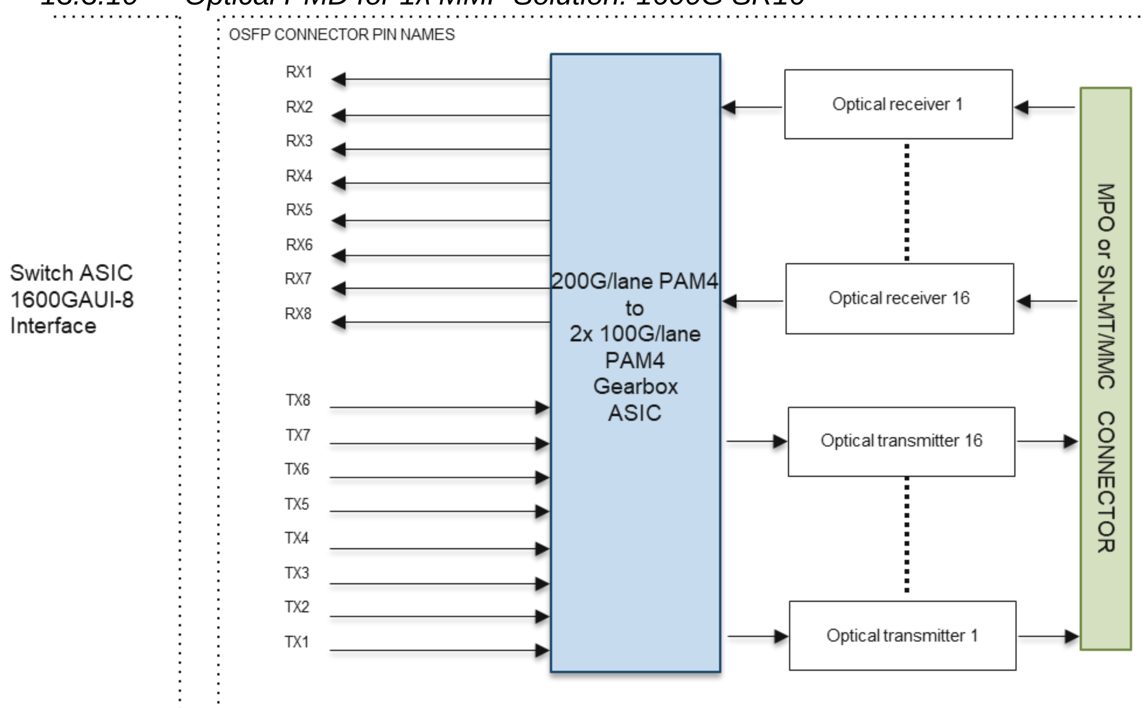


Figure 13-24: Block diagram, OSFP1600 optical PMD for 1600G SR16

13.3.11 Optical PMD for 4λ MMF Solution: 4x400G VR/SR SWDM4

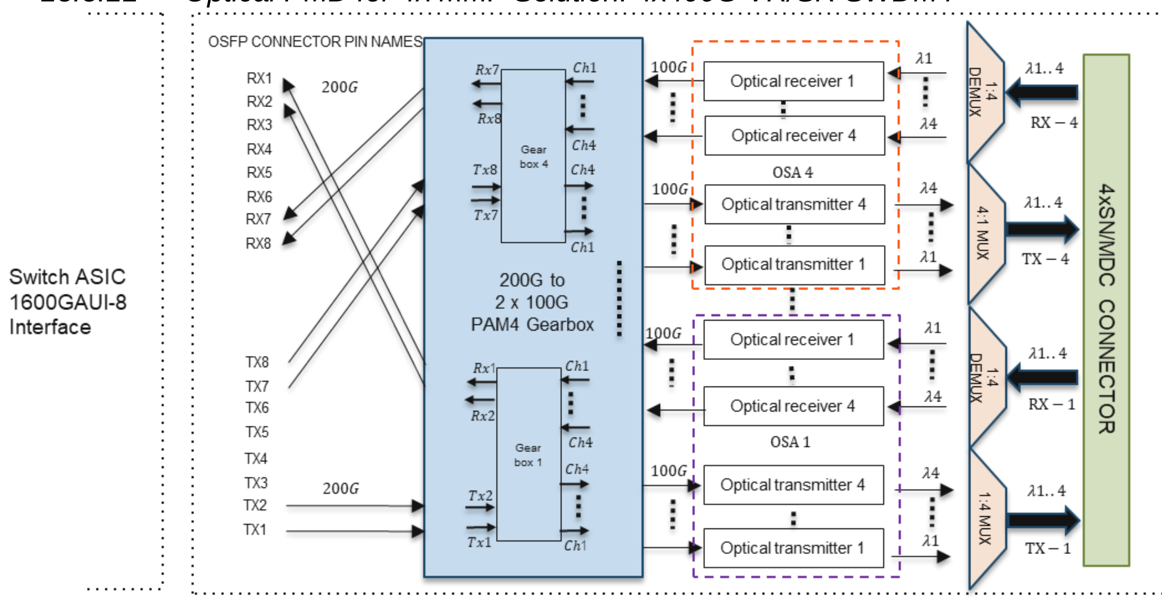


Figure 13-25: Block diagram, OSFP1600 optical PMD for 4x400G VR/SR SWDM4

13.3.12 Optical PMD for 2λ SMF/MMF Solution: 1600G-VR/SR8.2 & 1600G-DR8.2

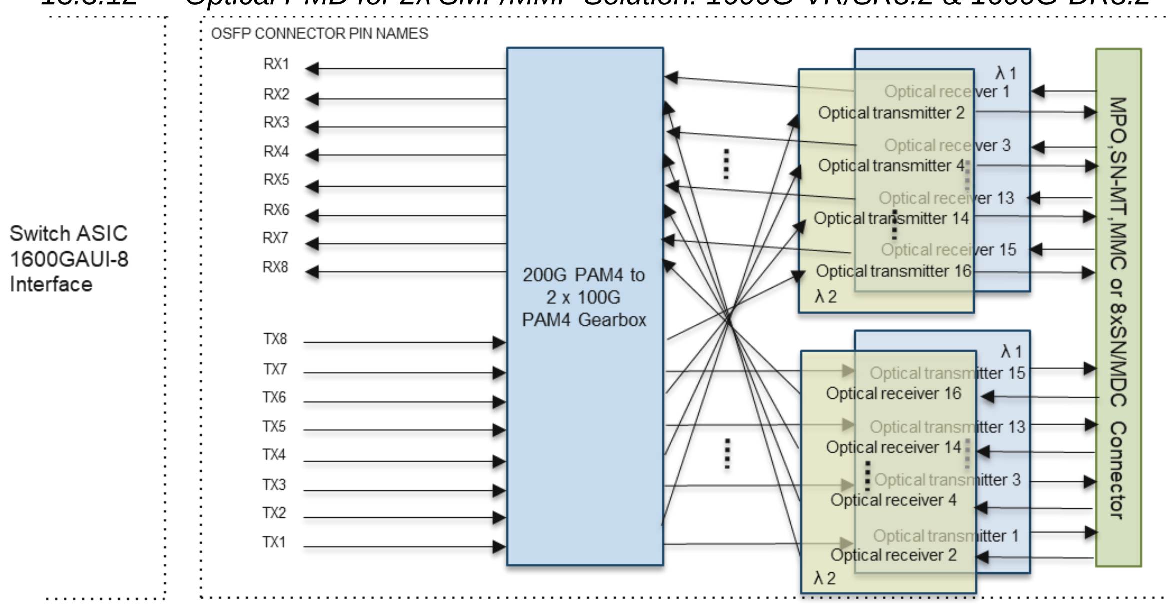


Figure 13-26: Block diagram, OSFP1600 optical PMD for 1600G-VR/SR8.2 & 1600G-DR8.2

13.4 OSFP Optical Interface

Optical interfaces that can be used for the OSFP modules are illustrated below. These interfaces are meant to be guidelines. The centerline of the optical interface to be aligned with module centerline within 2mm.

13.4.1 Duplex LC Optical Interface

Figure 13-27 shows channel orientation of the optical connector when a duplex LC connector as in IEC 61754-20 is used in an OSFP module. The view is from the front of a typical OSFP module, but actual OSFP module design of the heat sink or height of the optical connector may be different from shown.

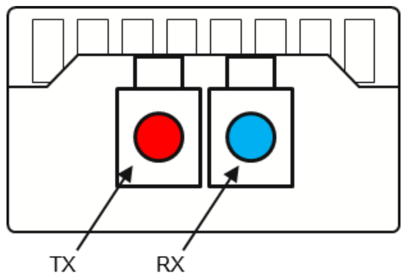


Figure 13-27: Optical receptacle and channel orientation for duplex LC connector

13.4.2 Dual Mini-LC Optical Interface

Figure 13-28 shows channel orientation of the optical connector when two Mini-LC connectors are used in side by side, consisting of dual mini-LC for an OSFP module.

Drawing below shows 11.35mm of pitch between the mini duplex LC connectors.

Note that the allowable size of the mating optical connector can be affected by the pitch of the ports on the module design and the optical connector design.

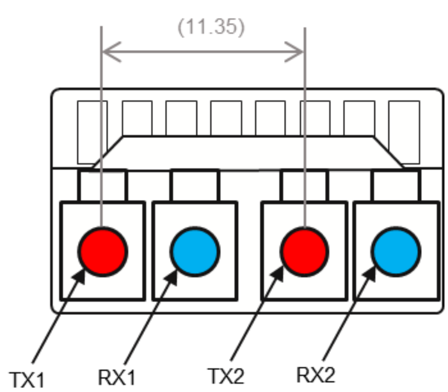


Figure 13-28: Optical receptacle and channel orientation for Dual Mini-LC

13.4.3 Dual Duplex LC Optical Interface

Figure 13-29 shows channel orientation of the optical connector when two duplex LC connectors are used as belly to belly, consisting of a dual duplex LC for an OSFP module. The connector should be spaced as in Figure 13-29. Duplex LC connector with dimensions as in the Figure 13-30 will fit into this spacing.

This configuration might be implemented in a Type 2 OSFP, as depicted in Figure 3-3 and Figure 13-29.

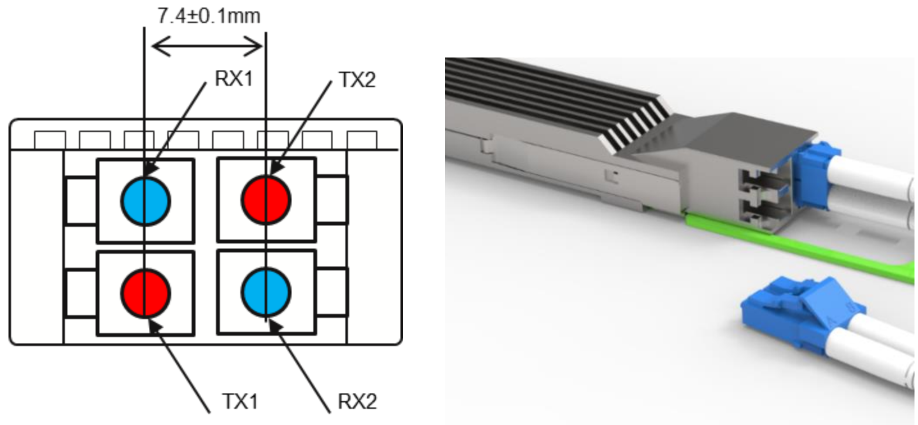


Figure 13-29: Optical receptacle and channel orientation for Dual LC, with an example

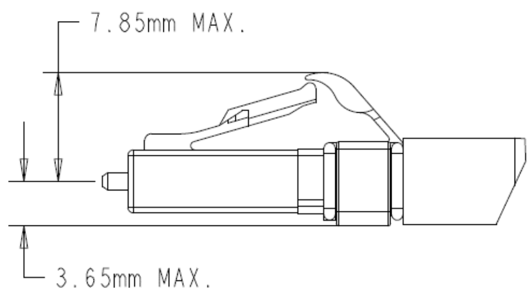


Figure 13-30: LC connector size per given belly-to-belly pitch

13.4.4 Dual CS® Optical Interface

Figure 13-31 shows channel orientation of the optical connector when a dual CS® connector is used in an OSFP module. Connector 1 (Tx1, Rx1) and connector 2 (Tx2, Rx2) are connected with two separate independent duplex fiber cables.

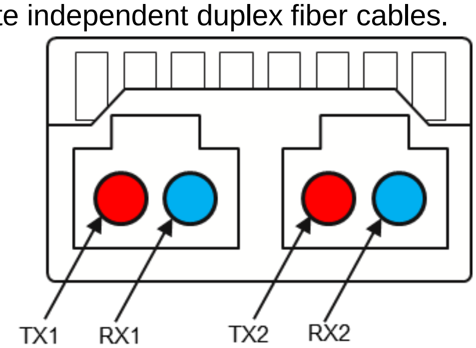


Figure 13-31: Optical receptacle and channel orientation for dual CS® connector

13.4.5 Dual MDC Optical Interface

Figure 13-32 shows channel orientation of the dual MDC connector for an OSFP module. Connector 1 and connector 2 are connected with two separate independent duplex fiber cables. MDC connectors are ganged, i.e. placed to side to side and release latch placed toward the top side of the module.

Figure 13-33 shows optical connector direction of the dual MDC connector for an OSFP module, when they are placed as stacked. The release latch direction is shown in the figure. Also, the TX/RX lane assignment for connector 1 and connector 2 are same with Figure 13-32.

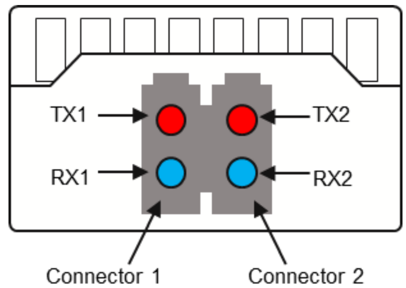


Figure 13-32: Optical receptacle and channel orientation for dual MDC connector (ganged)

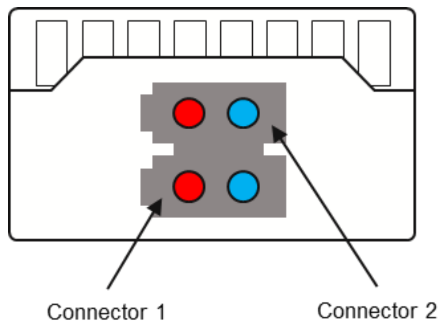


Figure 13-33: Optical receptacle for dual MDC connector (stacked)

13.4.6 Quad MDC Optical Interface

Figure 13-34 shows channel orientation of the optical connector when a quad MDC connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2), receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables. Figure 13-35 shows for the 400G-SR4.2.

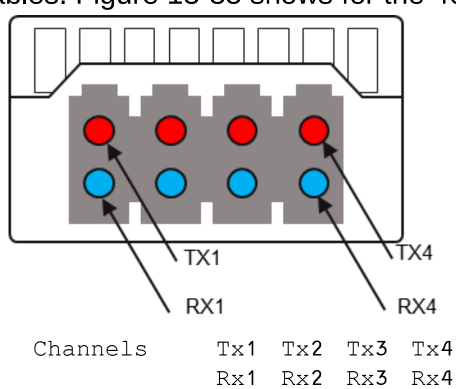
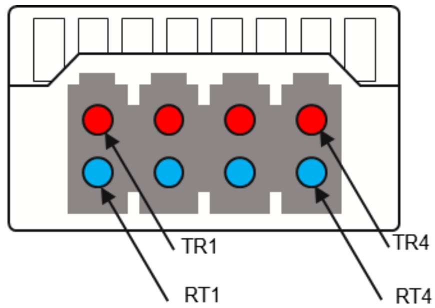


Figure 13-34: Optical receptacle and channel orientation for quad MDC connector for 400G DR-4



Quad MDC Ferrule Names	**TR1**	**TR2**	**TR3**	**TR4**
Signal Names (λ1)	Tx1	Tx3	Tx5	Tx7
Signal Names (λ2)	Rx2	Rx4	Rx6	Rx8
Quad MDC Ferrule Names	**RT1**	**RT2**	**RT3**	**RT4**
Signal Names (λ1)	Rx1	Rx3	Rx5	Rx7
Signal Names (λ2)	Tx2	Tx4	Tx6	Tx8

Figure 13-35: Optical receptacle and channel orientation for quad MDC connector for 400G-SR4.2

13.4.7 8 x MDC Optical Interface

8 MDC connectors can be placed to an OSFP module as in the Figure 13-36. This configuration might be implemented in a Type 3 OSFP, as depicted in the Figure 3-3 and Figure 13-37.

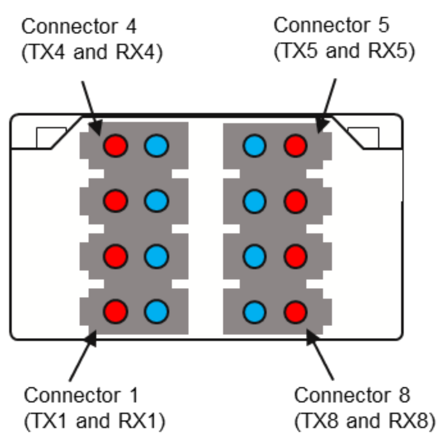


Figure 13-36: Optical receptacle and channel orientation for 8 x MDC connector

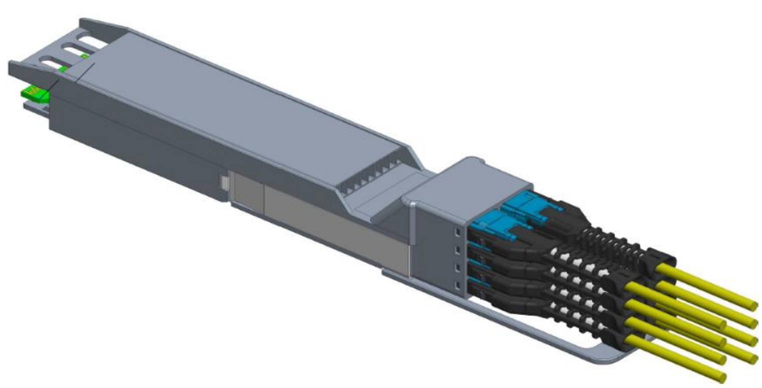


Figure 13-37: Example of a Type 3 OSFP with 8 x MDC connector

13.4.8 Dual SN® Optical Interface

Figure 13-38 shows channel orientation of the dual SN® connector for an OSFP module. Connector 1 and connector 2 are connected with two separate independent duplex fiber cables. SN® connectors are ganged, i.e. placed to side to side and release latch placed toward the top side of the module.

Figure 13-39 shows optical connector direction of the dual SN® connector for an OSFP module, when they are placed as stacked. The release latch direction is shown in the figure. Also, the TX/RX lane assignment for connector 1 and connector 2 are same with Figure 13-38.

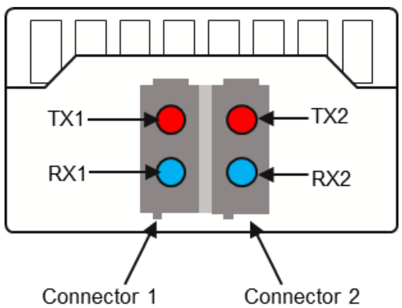


Figure 13-38: Optical receptacle and channel orientation for dual SN® connector (ganged)

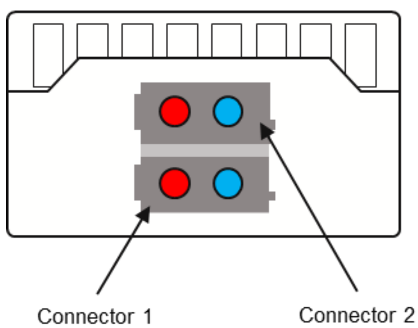
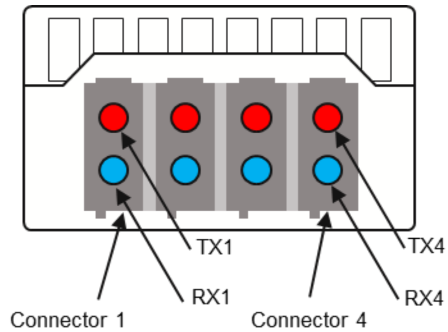


Figure 13-39: Optical receptacle for dual SN® connector (stacked)

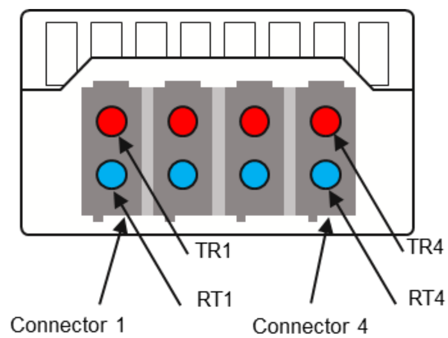
13.4.9 Quad SN® Optical Interface

Figure 13-40 and Figure 13-41 show channel orientation of the optical connector when a quad SN® connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2), receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables.



Channels				
	Tx1	Tx2	Tx3	Tx4
	Rx1	Rx2	Rx3	Rx4

Figure 13-40: Optical receptacle and channel orientation for Quad SN® connector for 400G-DR4



Quad SN Ferrule Names	**TR1**	**TR2**	**TR3**	**TR4**
Signal Names (λ1)	Tx1	Tx3	Tx5	Tx7
Signal Names (λ2)	Rx2	Rx4	Rx6	Rx8
Quad SN Ferrule Names	**RT1**	**RT2**	**RT3**	**RT4**
Signal Names (λ1)	Rx1	Rx3	Rx5	Rx7
Signal Names (λ2)	Tx2	Tx4	Tx6	Tx8

Figure 13-41: Optical receptacle and channel orientation for Quad SN® connector for 400G SR4.2

13.4.10 8 x SN® Optical Interface

8 SN® connectors can be placed to an OSFP module as in the Figure 13-42. This configuration might be implemented in a Type 3 OSFP, as depicted in the Figure 3-3.

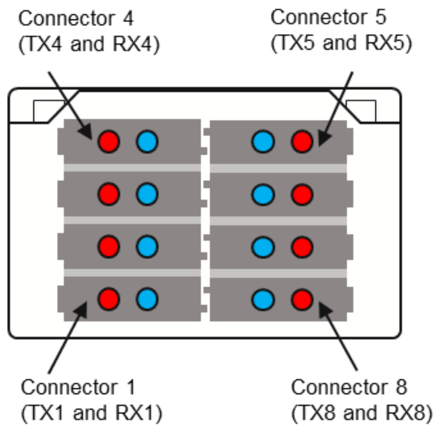


Figure 13-42: Optical receptacle and channel orientation for 8 x SN® connector

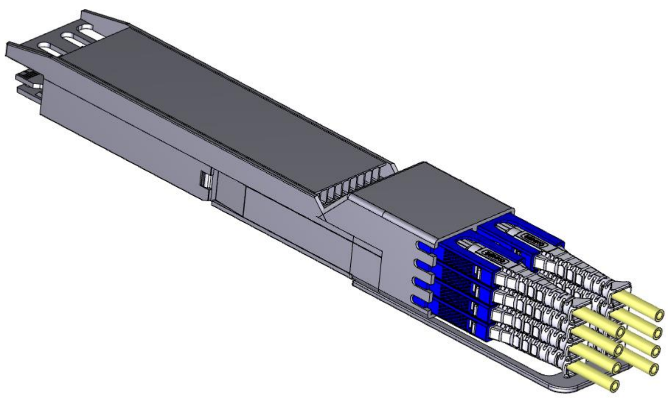
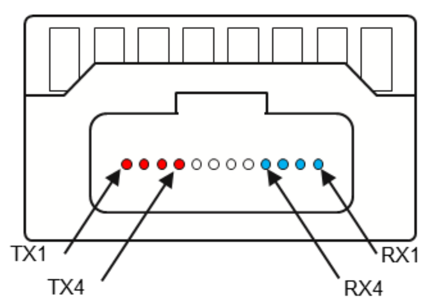


Figure 13-43: Example of a Type 3 module with 8 x SN® connector

13.4.11 MPO-12 Optical Interface

Figure 13-44 shows channel orientation of the optical connector when a male MPO-12 connector as in the IEC 61754-7-1 is used in an OSFP module for applications except 400G-SR4.2.

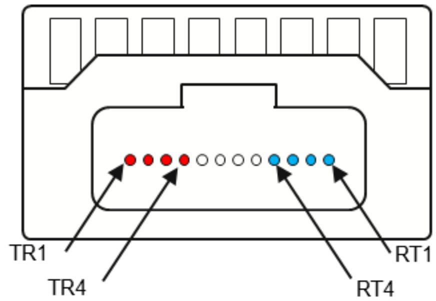



```
        Channels                Tx1 Tx2 Tx3 Tx4 x x x x Rx4 Rx3 Rx2 Rx1
   (x: unused position)
```

Figure 13-44: Optical receptacle and channel orientation for MPO-12 connector

Figure 13-45 shows the channel orientation of the optical connector and signal lane mapping when a male MPO-12 connector is used in an OSFP module for 400G-SR4.2 application.

There are two signals on two different wavelengths traveling on opposite directions inside each single fiber, as in the example shown in the section 13.1.3.



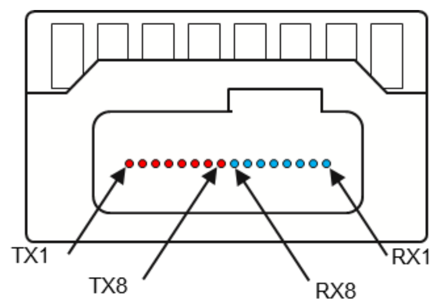
MPO Ferrule Names	TR1	TR2	TR3	TR4	x	x	x	x	RT4	RT3	RT2	RT1
Signal Names (λ1)	Tx1	Tx3	Tx5	Tx7	x	x	x	x	Rx7	Rx5	Rx3	Rx1
Signal Names (λ2)	Rx2	Rx4	Rx6	Rx8	x	x	x	x	Tx8	Tx6	Tx4	Tx2

Figure 13-45: Optical receptacle and channel orientation for MPO-12 for 400G-SR4.2

Fiber connectors that have the same footprint as the MPO connector, such as AirMT®, or 3M EBO-MP12/16, will use the same guideline for channel orientation as the MPO interface.

13.4.12 MPO-16 Optical Interface

Figure 13-46 shows channel orientation of the optical connector when a male MPO-16 connector as in the TIA-604-18 is used in an OSFP module.

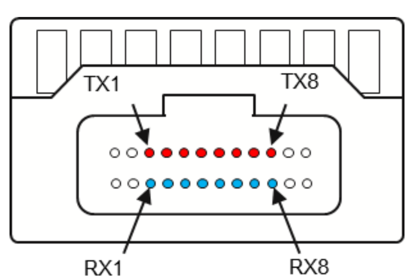


Channels	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1

Figure 13-46: Optical receptacle and channel orientation for MPO-16 connector

13.4.13 MPO-12 Two Row Optical Interface

Figure 13-47 shows channel orientation of the optical connector when a male MPO-12 Two Row connector as in the TIA-604-18 is used in an OSFP module.



Channels	x	x	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	x	x
(x: unused position)	x	x	Rx1	Rx2	Rx3	Rx4	Rx5	Rx6	Rx7	Rx8	x	x

Figure 13-47: Optical receptacle and channel orientation for MPO-12 Two Row connector

13.4.14 Dual MPO Optical Interface

Figure 13-48 shows channel orientation of the optical connector when dual MPO-12 connectors are used in an OSFP module. MPO-12 connectors, which channel assignment within the connector to be as in the Figure 13-44, will be used as depicted in the figure. Figure 13-48 also shows the spacing between the connectors. Figure 13-49 shows the size of the allowable connector in the given pitch. This configuration might be implemented in a Type 2 OSFP, as depicted in the Figure 3-3 and Figure 13-50.

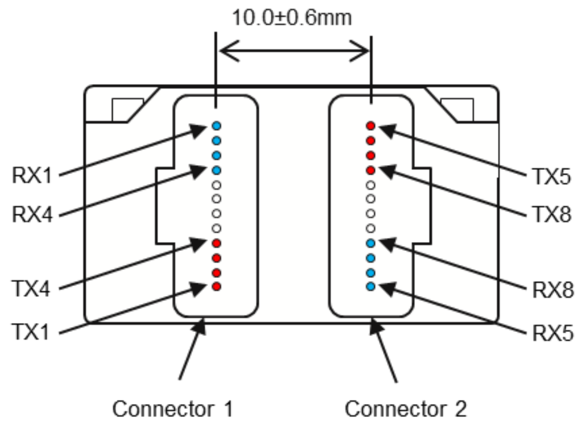


Figure 13-48: Optical receptacle and channel orientation for Dual MPO connector

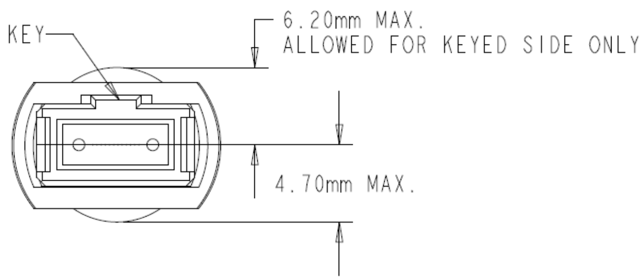


Figure 13-49: MPO connector size per given belly-to-belly pitch

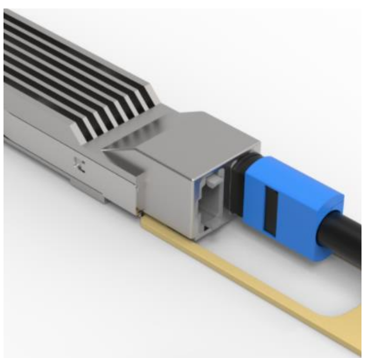


Figure 13-50: Example of an OSFP module with Dual MPO connector

13.4.15 MMC Optical Interface

Figure 13-51 shows channel orientation when a MMC connector with 16 fibers is used in an OSFP module.

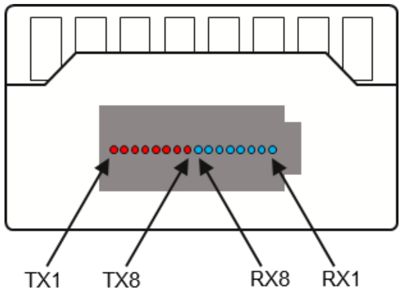


Figure 13-51: Optical receptacle and channel orientation for a MMC connector

Figure 13-52 shows channel orientation when a MMC connector with 2x12 fibers is used in an OSFP module.

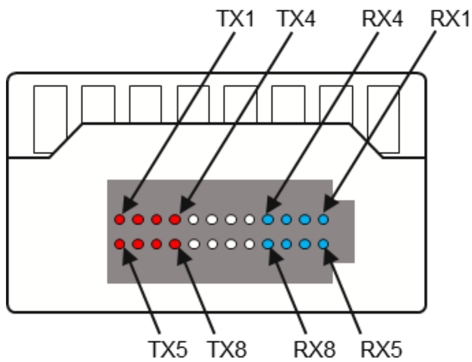


Figure 13-52: Optical receptacle and channel orientation for a MMC 2x12 connector

13.4.16 Dual MMC Optical Interface

Figure 13-53 and Figure 13-54 shows the channel orientation when dual MMC connectors are used in an OSFP module. Note that the MMC connector shown here is with 12 fibers.

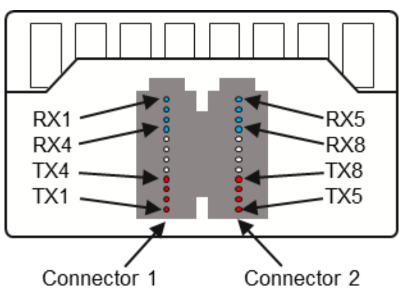


Figure 13-53: Optical receptacle and channel orientation for dual MMC (ganged)

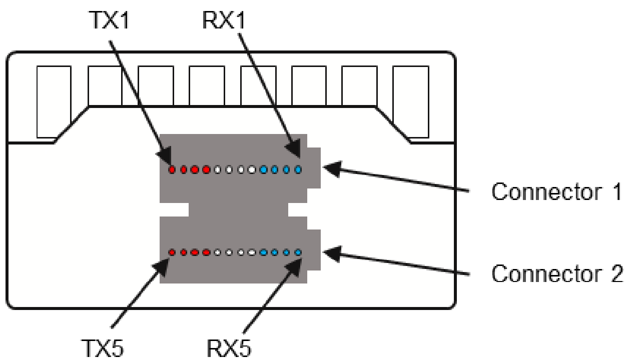


Figure 13-54: Optical receptacle and channel orientation for dual MMC (stacked)

13.4.17 SN-MT Optical Interface

Figure 13-55 shows channel orientation when a SN-MT connector with 16 fibers is used in an OSFP module.

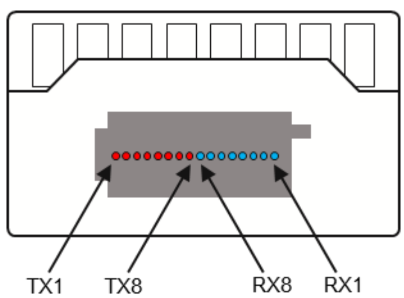


Figure 13-55: Optical receptacle and channel orientation for a SN-MT connector

Figure 13-56 shows channel orientation when a SN-MT connector with 2x12 fibers is used in an OSFP module.

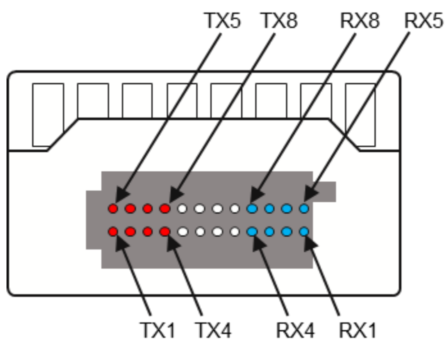


Figure 13-56: Optical receptacle and channel orientation for a SN-MT connector (2x12 fiber)

13.4.18 Dual SN-MT Optical Interface

Figure 13-53 and Figure 13-54 show the channel orientation when dual MMC connectors are used in an OSFP module. Note that the MMC connector shown here is with 12 fibers.

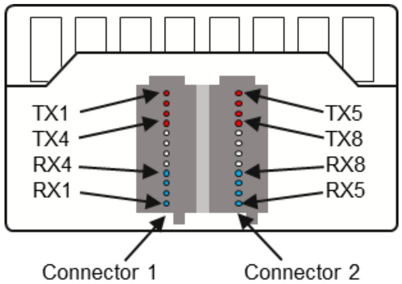


Figure 13-57: Optical receptacle and channel orientation for dual SN-MT (ganged)

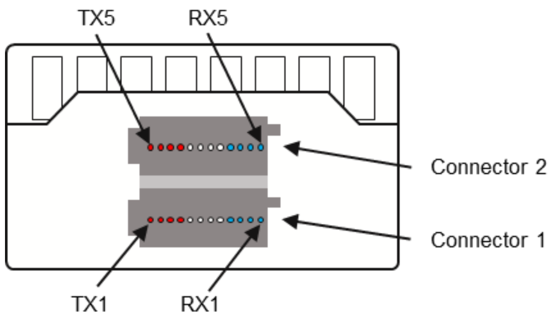


Figure 13-58: Optical receptacle and channel orientation for dual SN-MT (stacked)

13.4.19 MXC Optical Interface

Figure 13-59 shows channel orientation of a MXC connector with 16 fibers when it is used in the OSFP module.

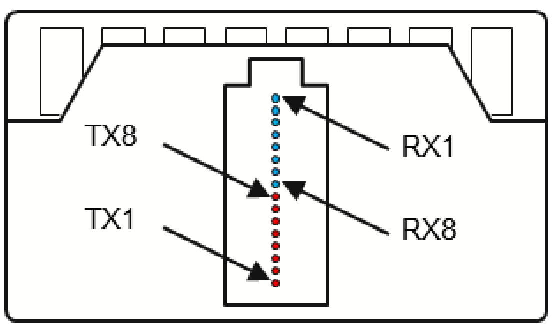


Figure 13-59: Optical receptacle and channel orientation for MXC connector

13.4.20 Dual MXC Optical Interface

Figure 13-60 shows channel orientation of the optical connector when dual MXC connectors are used in an OSFP module. Connector 1 will be used for the first half of the channels of the module (RX1~4 and TX 4~1) while the Connector 2 will be used for the second half of the channels of the module (RX5~8 and TX 8~5). Figure 13-61 shows an example of OSFP with dual MXC connectors. This configuration might be implemented in a Type 2 OSFP, as depicted in the Figure 3-3.

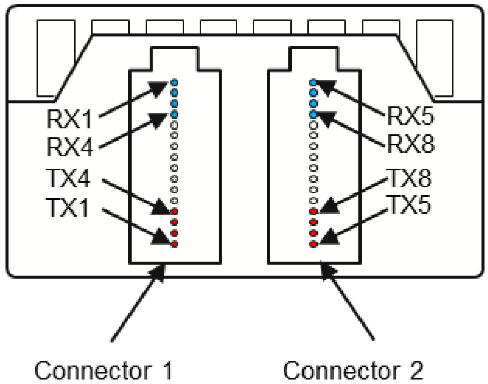


Figure 13-60: Optical receptacle and channel orientation for Dual MXC connector

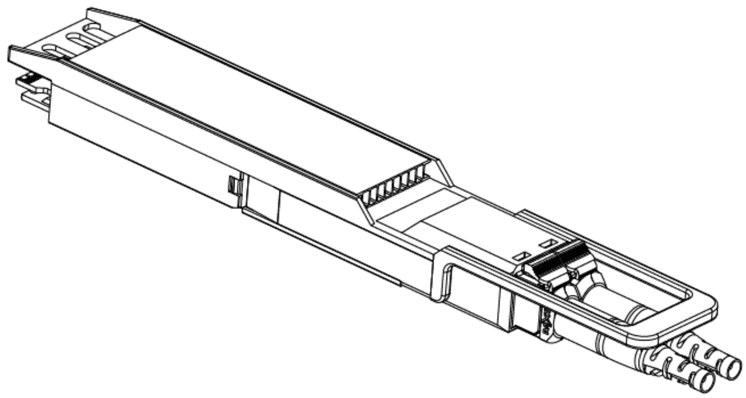


Figure 13-61: Example of an OSFP module with Dual MXC connector

14 Electrical Interface

14.1 Module Electrical Connector

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in Figure 14-1. It provides 16 contacts for 8 differential pairs of high-speed transmit signals, 16 contacts for 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

The chassis ground (case common) of the OSFP module shall be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module. When an OSFP module is not installed, the signals to the connector within the unused cage should be disabled to minimize electromagnetic interference (EMI) emissions.

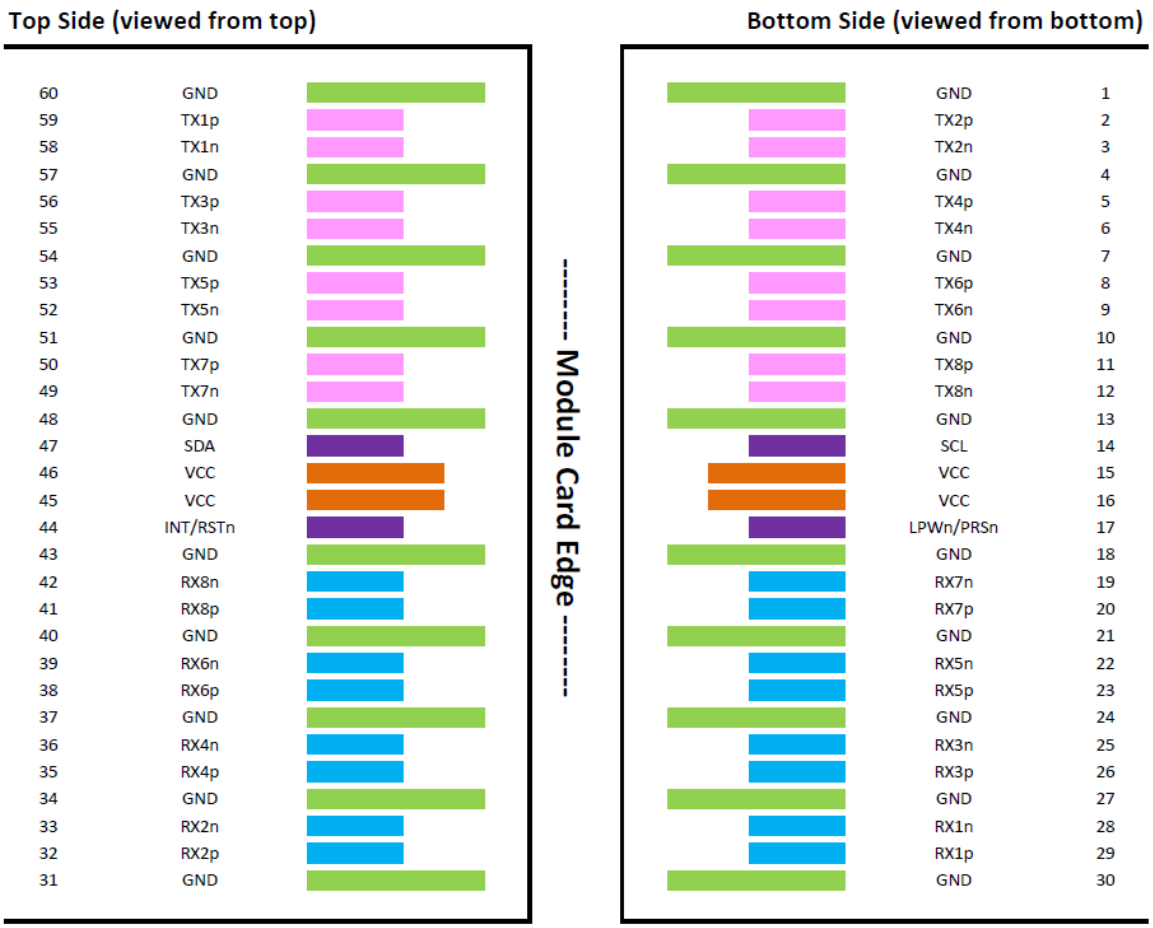


Figure 14-1: OSFP module pinout

14.2 Pin Descriptions

Table 14-1: OSFP module signal pin descriptions

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in section 14.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in section 14.5.2
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

14.3 Pin List

Table 14-2: OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

14.4 High-Speed Signals

The high-speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in port configurations of either a single 8-lanes, dual 4-lanes, quad 2-lanes or 8 individual lanes depending on the capability of the host ASIC.

1.6TAUI-8 mode provides 8 differential lanes using 224G-PAM4 signaling operating at 106.25 Gbaud. This results in 8 lanes of 200Gb/s for a total of 1.6Tb/s. This mode allows for connection to PMD configurations of 1x1.6T, 2x800G, 4x400G, or 8x200G.

800GAUI-8 mode provides 8 differential lanes using 112G-PAM4 signaling operating at 53.125 Gbaud. This results in 8 lanes of 100Gb/s for a total of 800Gb/s. This mode allows connection to PMD configurations of 1x800G, 2x400G, 4x200G or 8x100G.

400GAUI-8 mode provides 8 differential lanes using 56G-PAM4 signaling operating at 26.5625 Gbaud. This results in 8 lanes of 50Gb/s for a total of 400Gb/s. This mode allows connection to PMD configurations of 1x400G, 2x200G, 4x100G or 8x50G.

Dual CAUI-4 mode provides 8 differential lanes using 25G-NRZ signaling operating at 25.78125 Gbaud. This results in 8 lanes of 25Gb/s for a total of 200Gb/s. This mode allows connection to PMD configurations of 2x100G, 4x50G or 8x25G.

The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE 802.3ck and CEI-56G-VSR-PAM4 as defined in OIF-CEI-05.2 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

The lane assignments in Table 14-3 shall be used for the different PMD configurations.

Table 14-3: High-speed signal lane mapping

(*L means Lane, L1 means Lane 1 in the port.)

<table>
<tr><th rowspan="2">PMD Configuration</th><th colspan="8">Transmit and Receive Lane Assignments</th></tr>
<tr><th>L1</th><th>L2</th><th>L3</th><th>L4</th><th>L5</th><th>L6</th><th>L7</th><th>L8</th></tr>
<tr><td>1x1.6T (224G-PAM4)
1x800G (112G-PAM4)
1x400G (56G-PAM4)</td><td colspan="8">Port 1</td></tr>
<tr><td rowspan="2">2x800G (224G-PAM4)
2x400G (112G-PAM4)
2x200G (56G-PAM4)
2x100G (25G-NRZ)</td><td colspan="4">Port 1</td><td colspan="4">Port 2</td></tr>
<tr><td>L1*</td><td>L2</td><td>L3</td><td>L4</td><td>L1</td><td>L2</td><td>L3</td><td>L4</td></tr>
<tr><td rowspan="2">4x400G (224G-PAM4)
4x200G (112G-PAM4)
4x100G (56G-PAM4)
4x50G (25G-NRZ)</td><td colspan="2">Port 1</td><td colspan="2">Port 2</td><td colspan="2">Port 3</td><td colspan="2">Port 4</td></tr>
<tr><td>L1</td><td>L2</td><td>L1</td><td>L2</td><td>L1</td><td>L2</td><td>L1</td><td>L2</td></tr>
<tr><td>8x200G (224G-PAM4)
8x100G (112G-PAM4)
8x50G (56G-PAM4)
8x25G (25G-NRZ)</td><td>Port 1</td><td>Port 2</td><td>Port 3</td><td>Port 4</td><td>Port 5</td><td>Port 6</td><td>Port 7</td><td>Port 8</td></tr>
</table>

14.5 Low-Speed Signals

There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals. LPWn/PRSn and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

14.5.1 SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I^{2}C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I^{2}C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I^{2}C Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- Optional - I3C Single Data Rate (SDR) ≤ 12.5 Mbit/s

The host shall default to using 100 kbit/s standard-mode I^{2}C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I^{2}C Fast-mode, I^{2}C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I^{2}C-bus specification or Single Data Rate mode as defined in the Specification for I3C.

14.5.2 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host, and also allows the host to reset the module. The circuit shown in Figure 14-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-high signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 14-2 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INT signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

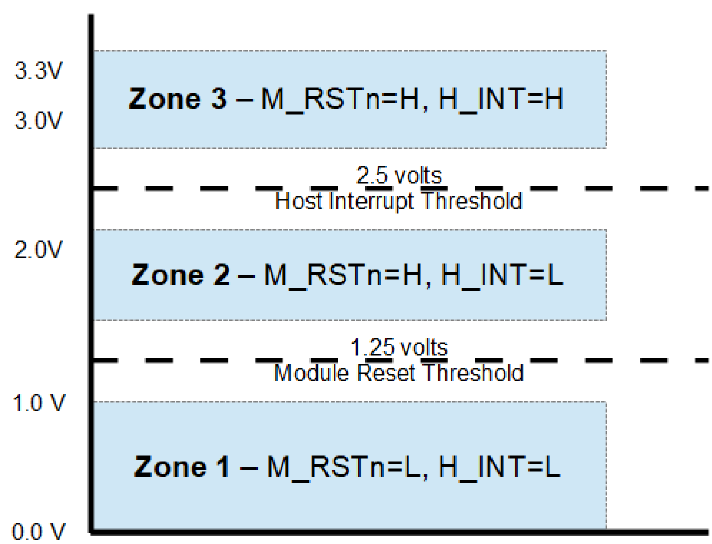


Figure 14-2: INT/RSTn voltage zones

- Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INT=Low). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 14-4.
- Zone 2 – Normal operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INT=Low). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 14-4.
- Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INT=High). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 14-4.

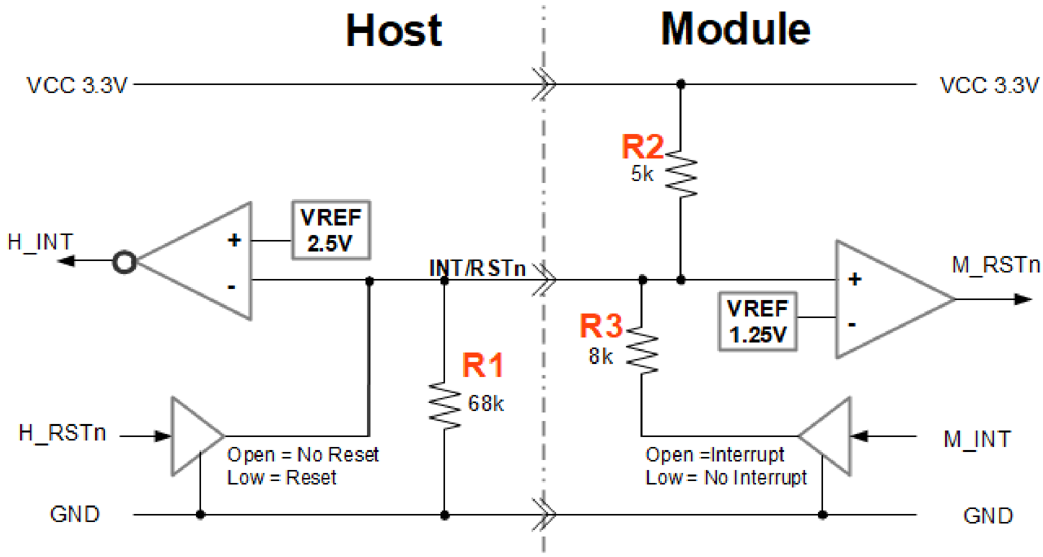


Figure 14-3: INT/RSTn circuit

Table 14-4: INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INT	2.500	2.475	2.525	Volts	Precision voltage reference for H_INT
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

The description of the H_INT signal has been updated starting with MSA revision 5.0. The functionality and implementation have not changed but the description has been updated to use the non-inverted signal (H_INT) instead of the inverted signal (H_INTn). This makes the polarity of the interrupt signal the same between the module (M_INT) and host (H_INT) for better clarity. This is purely a description change with no change to functionality. Host implementations with an inverted interrupt signal are fully OSFP MSA specification compliant.

14.5.3 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 14-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 14-4 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

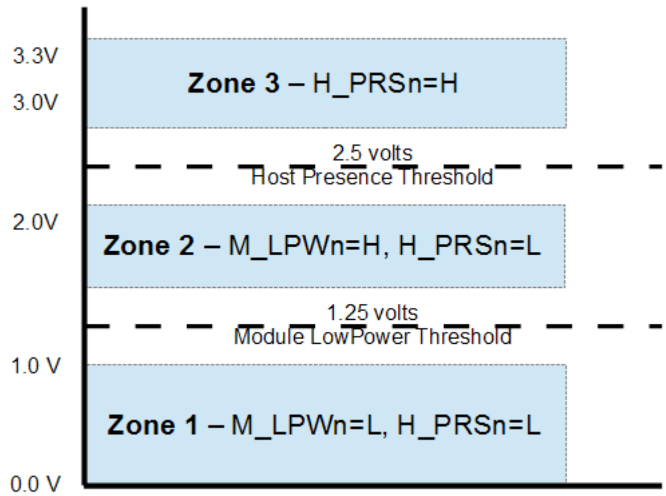


Figure 14-4: LPWn/PRSn voltage zones

- Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 14-5.
- Zone 2 – High Power mode – Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 14-5.
- Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 14-5.

Module Removal – If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the module shall assert Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp in Table 14-7. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level then 3.3V LVCMOS is preferred.

For very low cost modules, such as DAC, the voltage comparator on the module may be omitted and the LPWn/PRSn pin shall in that case be tied to GND in the module. This type of module may only be used for low power mode (Power Class 1).

The module transmitters must be disabled when in Low Power mode. This ensures Power Class 1 and also provides a fast hardware shut down mechanism for applications such as redundancy switch-over. In addition, software controlled transmitter disable is provided by the TX Disable register via the I^{2}C interface.

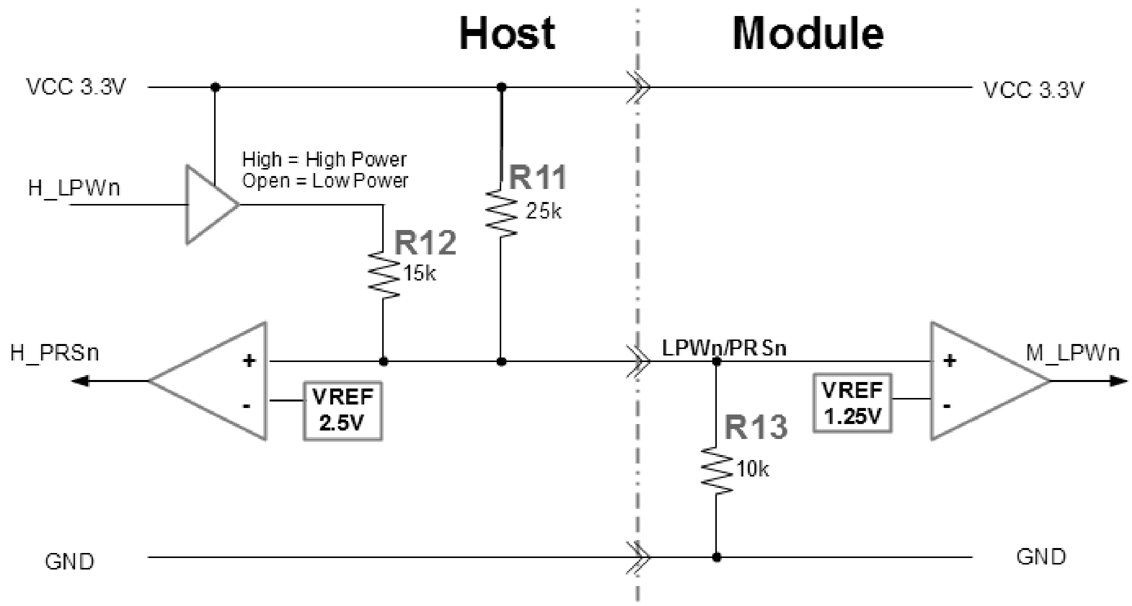


Figure 14-5: LPWn/PRSn circuit

Table 14-5: LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

14.5.4 Timing for Control and Status Functions

The QSFP-DD specification should be followed for any timing of control and status functions that have not been defined in this specification.

14.5.5 OSFP Module Power Up Behavior

The OSFP module shall power up when system power is enabled or on module insertion or on VCC power enable to the module. Once powered, the module shall either wait in Low Power mode or enter High Power mode based on the state of the Reset signal, Low Power signal and ForceLowPwr bit of the module. The ForceLowPwr bit default is pre-programmed in the module by the manufacturer and typically would be set to 0. The host can change the ForceLowPwr bit after power up but it shall return to its pre-programmed default when the module is placed in reset or power cycled. The Reset and Low Power signals are described in sections 14.5.2 and 14.5.3. The ForceLowPwr bit is defined in the OSFP Management Interface Specification.

The table below shows the module power up state based on Low Power and ForceLowPwr. If LPWn=0 then the module shall go into low power mode and transmitters disabled. If ForceLowPwr=0 and LPWn=1 then the module shall immediately enable transmitters. If ForceLowPwr=1 and LPWn=1 then the module shall wait in Low Power mode until the host clears the ForceLowPwr bit for the module to enable transmitters.

Table 14-6: Power up behavior

Module State	ForceLowPwr = 0	ForceLowPwr = 1
Low Power asserted (LPWn = 0)	Low Power Mode (transmitters Disabled)	Low Power Mode (transmitters Disabled)
Low Power de-asserted (LPWn = 1)	Operational (transmitters Enabled*)	Low Power Mode (transmitters Disabled)

*The host may use the management interface to alter this default behavior

14.5.6 OSFP Module Reset Behavior

Reset is a hardware signal from the INT/RSTn pin as defined in section 14.5.2. Asserting Reset overrides all other hardware and software controls and forces the module into the Reset state. This includes forcing Low Power mode and disabling transmitters.

14.6 Power

+3.3V power is delivered to the module via 4 power pins (VCC). These 4 power pins shall be connected together on the module and also together on the host. Each power pin allows up to 2.5 Amps for a total of 10.0 Amps. This enables a maximum power in excess of 30 Watts.

The specification of the OSFP host board's power supply noise output is in accordance with SFF-8679 revision 1.8.2 section 6.6.4. That of the OSFP module's noise output is in accordance with SFF-8679 revision 1.8.2 section 6.6.5. Finally, the OSFP module's power supply tolerance specification is in accordance with SFF-8679 revision 1.8.2 section 6.6.6. There are 8 power classes defined as shown in Table 14-8. All modules in reset or the default low power mode must comply with Power Class 1. High power mode enables the module to draw power up to its advertised power class and may be conditionally enabled by the host. The host may read the module power class register to know the power class of the module before or after enabling high power mode. The module shall not exceed the power class it identifies for itself.

Transition between low and high power mode is controlled by the M_RSTn (reset) signal, M_LPWn (low power mode) signal and ForceLowPwr bit. The module shall remain in or transition to low power mode when M_LPWn or M_RSTn are asserted or the ForceLowPwr bit is set. While in low power mode, active modules shall also disable transmitters. The module may transition to high power mode once M_RSTn and M_LPWn are deasserted and the ForceLowPwr bit is cleared.

The specifications of Table 14-7 and Table 14-8 are for the combined power of all 4 power pins. The measurement location for these specifications is at the OSFP connector VCC pins on the host board.

Table 14-7: OSFP power specification

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.201	3.300	3.465	V
Voltage drop across mated connector (Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV
Total current for Vcc pins (1)	Icc_module			10.0	A
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (2)	I_didt			100	mA/µs
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs

(1) Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

(2) The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power and high-power to low-power.

Table 14-8: OSFP power classes

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Low Power Mode – M_LPWn or M_RSTn asserted or ForceLowPwr					
Power consumption	P_lp			2	W
Instantaneous peak current at hot plug	Icc_ip_lp			800	mA
Sustained peak current at hot plug	Icc_sp_lp			666	mA
Steady state current (1)	Icc_lp			637	mA
Power Class 1 module (high power mode)					
Power consumption	P_1			1.5	W
Instantaneous peak current at hot plug	Icc_ip_1			600	mA
Sustained peak current at hot plug	Icc_sp_1			500	mA
Steady state current (1)	Icc_1			478	mA
Power Class 2 module (high power mode)					
Power consumption	P_2			3.5	W
Instantaneous peak current at high power enable	Icc_ip_2			1400	mA
Sustained peak current at high power enable	Icc_sp_2			1167	mA
Steady state current (1)	Icc_2			1116	mA
Power Class 3 module (high power mode)					
Power consumption	P_3			7	W
Instantaneous peak current at high power enable	Icc_ip_3			2800	mA
Sustained peak current at high power enable	Icc_sp_3			2333	mA
Steady state current (1)	Icc_3			2233	mA
Power Class 4 module (high power mode)					
Power consumption	P_4			8	W
Instantaneous peak current at high power enable	Icc_ip_4			3200	mA
Sustained peak current at high power enable	Icc_sp_4			2666	mA
Steady state current (1)	Icc_4			2552	mA
Power Class 5 module (high power mode)					
Power consumption	P_5			10	W
Instantaneous peak current at high power enable	Icc_ip_5			4000	mA
Sustained peak current at high power enable	Icc_sp_5			3333	mA
Steady state current (1)	Icc_5			3190	mA
Power Class 6 module (high power mode)					
Power consumption	P_6			12	W
Instantaneous peak current at high power enable	Icc_ip_6			4800	mA
Sustained peak current at high power enable	Icc_sp_6			4000	mA
Steady state current (1)	Icc_6			3828	mA
Power Class 7 module (high power mode)					
Power consumption	P_7			14	W
Instantaneous peak current at high power enable	Icc_ip_7			5600	mA
Sustained peak current at high power enable	Icc_sp_7			4666	mA
Steady state current (1)	Icc_7			4466	mA
Power Class 8 module (high power mode)					
Power consumption	P_8 (2)			>14	W
Instantaneous peak current at high power enable	Icc_ip_8			P_8 * 400	mA
Sustained peak current at high power enable	Icc_sp_8			P_8 * 333	mA
Steady state current (1)	Icc_8			7600	mA

(1) Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

(2) Power consumption P_8 is readable from the module Max Power register as defined in the Management Specification.

As a reference, the maximum power allowed in the previous revisions in the OSFP MSA are listed in Table 14-9.

Table 14-9: OSFP power summary per MSA revision

OSFP MSA Rev	Max Current	Max Power (at 3.3V nominal)
1.0	6 A	19.8 W
2.0	6.4 A	21.1 W
3.0	6.4 A	21.1 W
4.0	10 A	33.0 W
5.0	10 A	33.0 W

14.6.1 Power Filter

Figure 14-6 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering, then the same filter characteristics as this example filter shall be met.

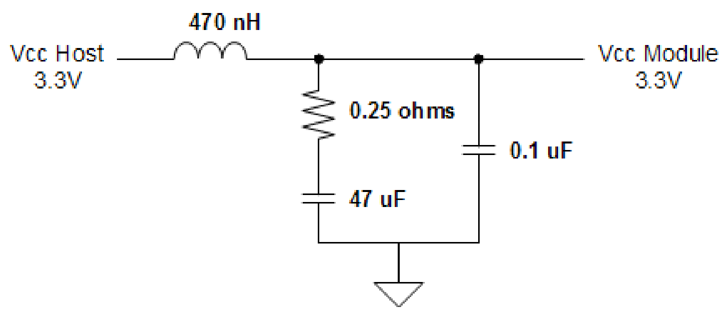


Figure 14-6: Host board power filter circuit

14.6.2 Power Electronic Circuit Breaker (optional)

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

14.7 OSFP Host Board and Module Block Diagram

Figure 14-7 is an example block diagram of the host board's connections to the OSFP module.

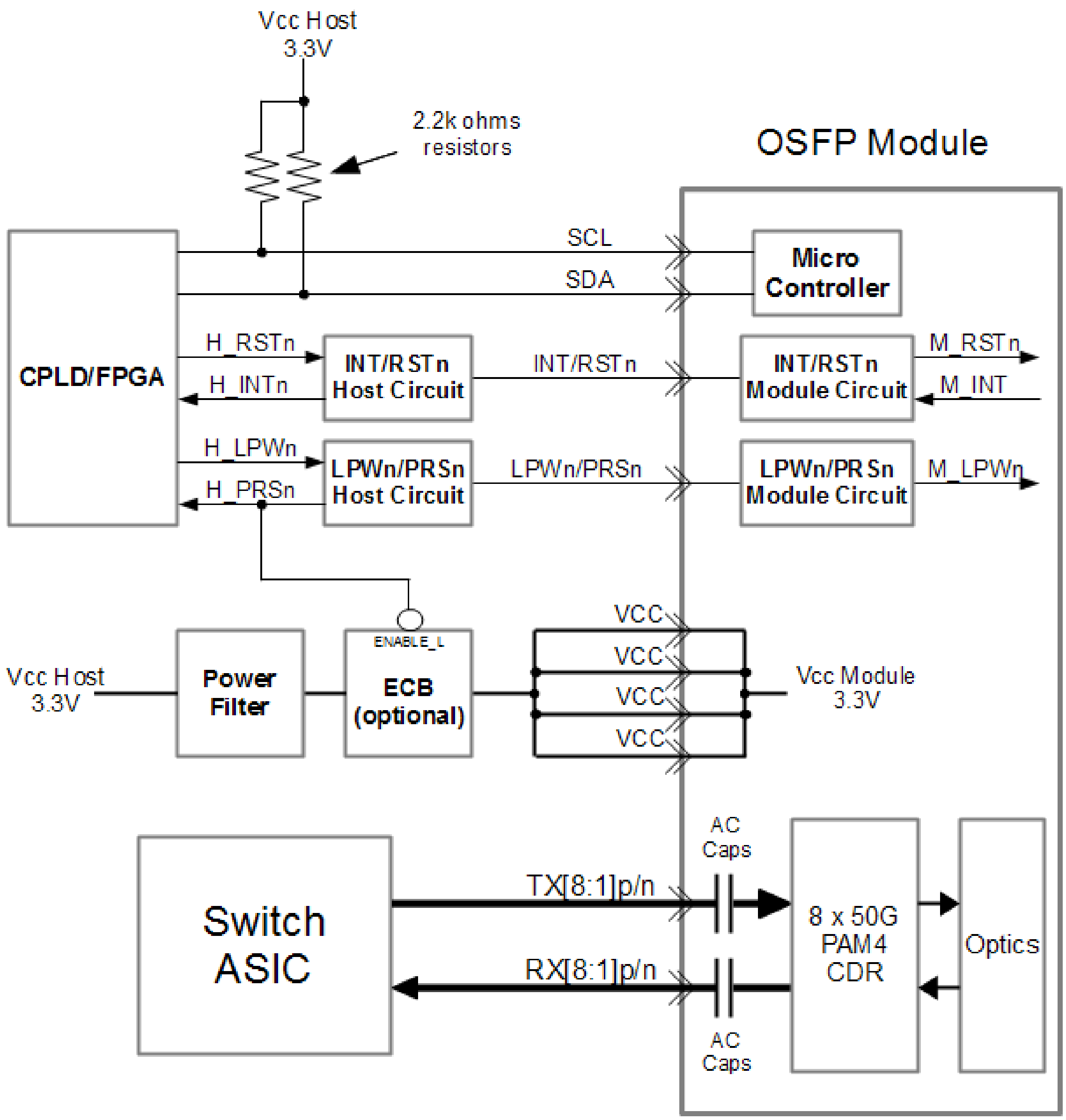


Figure 14-7: Host board and Module block diagram

14.8 Electrostatic Discharge (ESD)

Where ESD performance is not otherwise specified, the OSFP module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

The OSFP module and host high-speed signal, low-speed signal and power contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

Appendix A. OSFP Module LED (Informative)

A.1 LED Indicator and its Scheme

An OSFP module may have one or more LEDs at the front for use as a status indicator. In cases where a single LED is used for status indication of a multi-channel OSFP module, a green/yellow bi-color LED is recommended. In such case, the LED should light solid green when all channels of the module are operational and solid yellow when all channels are disabled. In cases where some channels are operational and some have fault conditions, a repeating pattern of LED flashing as outlined in Table A-1 is recommended.

Table A-1: Suggested OSFP LED signaling scheme for multiple channel modules

LED Status	Indication
On for 0.22 seconds	Green indicates channel 1 operational; Yellow indicates channel 1 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
On for 0.22 seconds	Green indicates channel 2 operational; Yellow indicates channel 2 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
…. Pattern repeats to final (*n*th) port	…
LED off for 1.76 seconds	Long pause for clear separation before pattern repeats from the beginning.

Appendix B. OSFP Pull Tab Length (Informative)

B.1 OSFP Pull Tab Length

An OSFP module may have a pull tab. Figure B-1 and B-2 show reference pull tab lengths with respect to the module positive stop. The pull tab should not interfere with optical plugs used in the section 13.4. Note that this does not apply to passive copper cables.

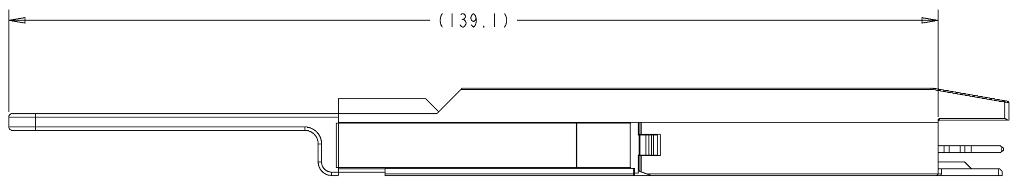


Figure B-1: OSFP pull tab length, from the stop feature

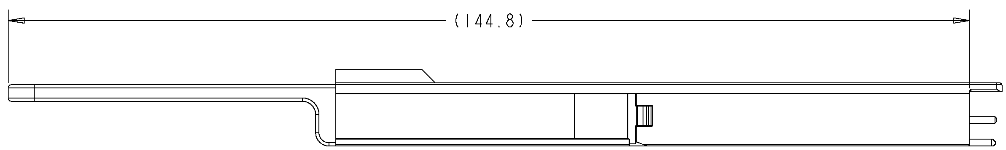


Figure B-2: OSFP-RHS pull tab length, from the stop feature

Appendix C. OSFP with Heatsink on the Bottom

C.1 Bottom Heatsink Dimensions

The OSFP module is permitted to have an integrated heatsink on the bottom side for improved thermal control. Figure C-1 and Figure C-2 depict the OSFP module bottom side integrated heatsink design and fin placement. Figure C-3 provides the fin design details. The fin design and placement are consistent with the open top heatsink design specified in section 3.4, to comply with the EMI cage finger in section 5.3.

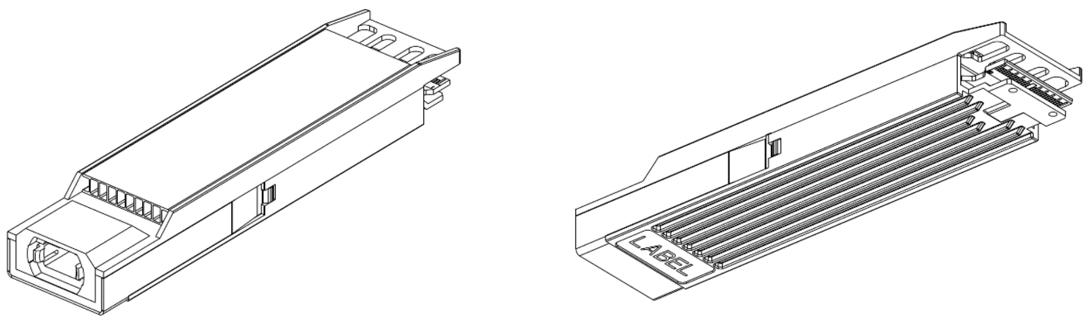


Figure C-1: OSFP module with bottom heatsink

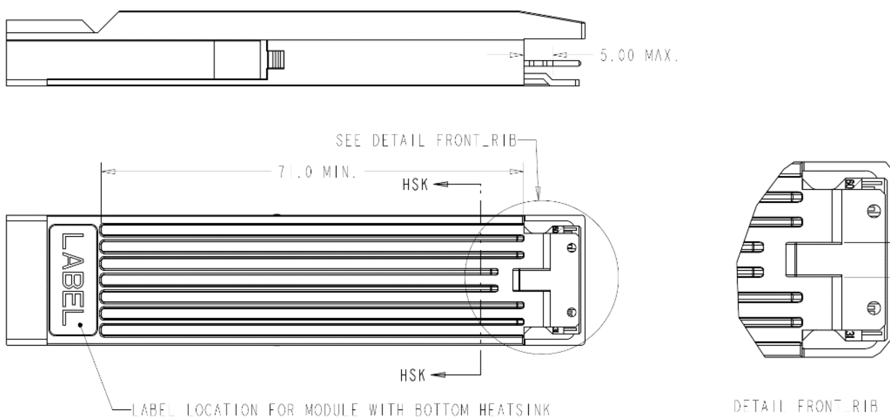


Figure C-2: OSFP with bottom heatsink, shape of the back

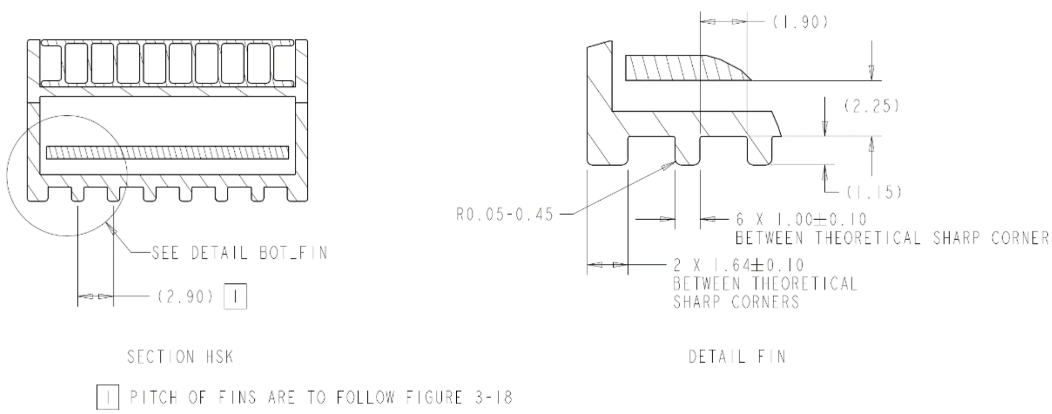


Figure C-3: Bottom heatsink fin pitch

Appendix D. Latch Release Width Inspection Fixture

D.1 Example of the Latch Release Width Inspection Fixture

In Figure 3-27 and Figure 4-8, maximum OSFP module latch release is specified. The maximum width between two opposite latch release can be measured in a virtual condition (as in the Figure 3-27), or whether the module can pass the cavity of the width of 22.78mm which is functional requirement for the OSFP module. Both methods are fine.

Figure D-1 shows a fixture, which can accept an OSFP module. The inlet has 22.78mm width. Figure D-2 shows the usage of the fixture; when the module placed to the fixture which have 45 degrees to the ground, the module is accepted if the module can be drop to the fixture with gravity or with up to 10N of the additional force.

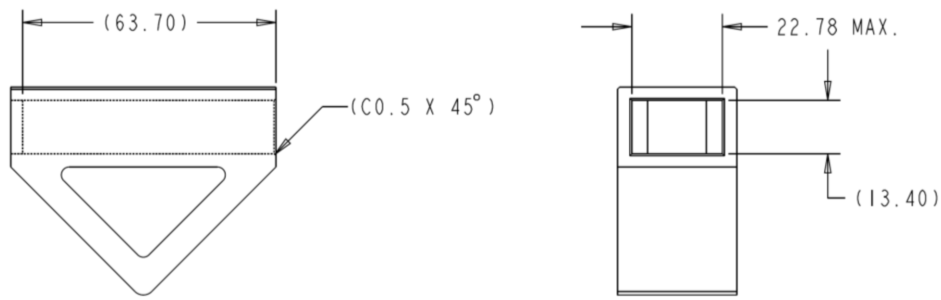


Figure D-1: Latch release width fixture

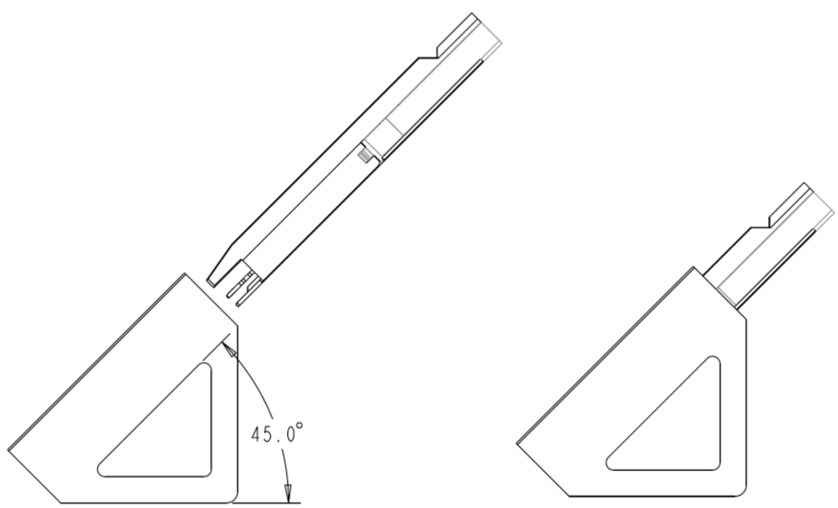


Figure D-2: Usage of the latch release width fixture

Appendix E. Cage Flap Location Inspection Gauge

E.1 Example of the Cage Flap Location Inspection Gauge

In Figure 6-5 and Figure 12-22, the location of the cage flap with respect to the cage positive stop is specified. The location dimension can be measured with a physical gauge or measured under unmated condition and then converted for the flap under mated height (flap deflected to 0.95 mm symmetrically). There is no restriction on how to inspect and measure the flap location if it meets the specification at deflected position as described in Figure 6-5.

A reference design of a gauge tool is shown as in the Figure E-1. Gauge for the OSFP1600-RHS differ only on its thickness. Figure E-2 shows how the gauge can be used. While the dimension “A” reproduces the mated condition, Dimension B will center align the gauge inside the cage.

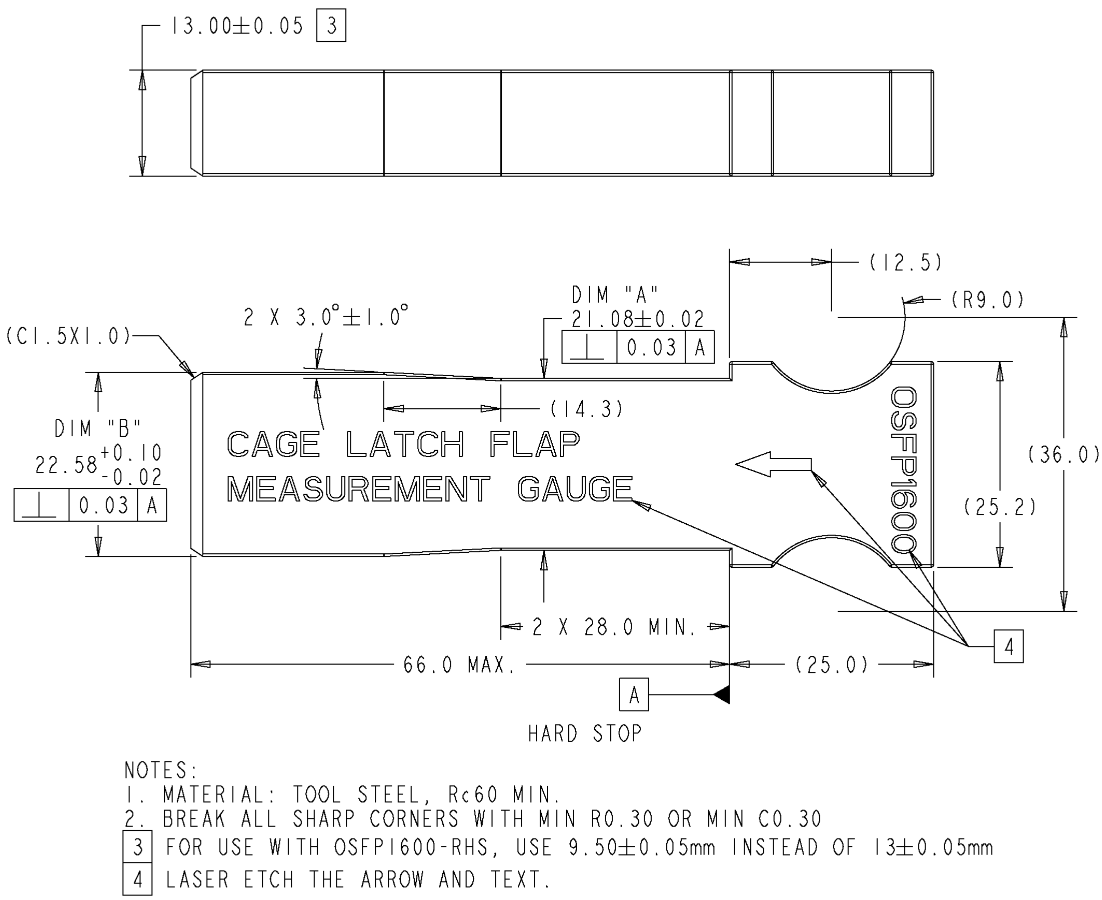


Figure E-1: OSFP1600 Cage flap location inspection gauge (Reference)

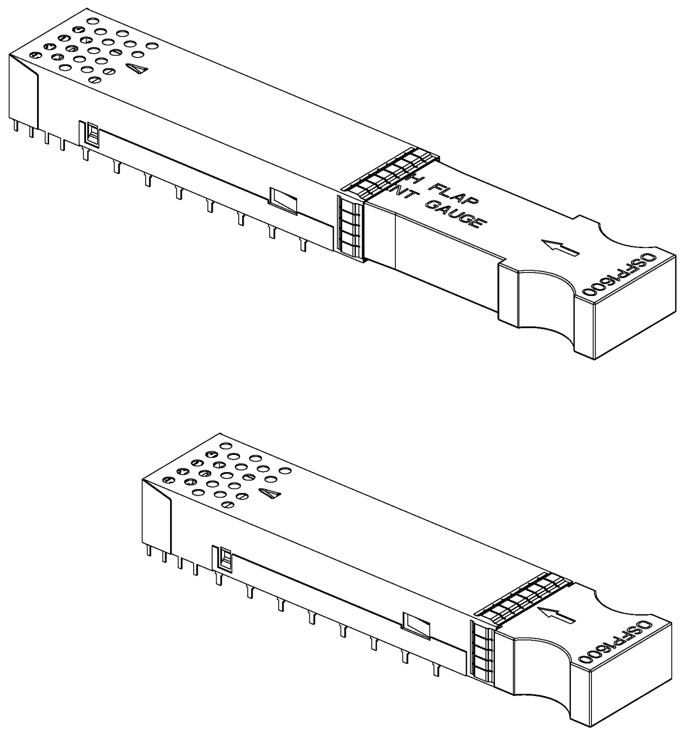


Figure E-2: Usage of cage flap location gauge

Appendix F. Cross-Incompatibility of OSFP and OSFP-XD

OSFP-XD module is a pluggable module with 16 lanes, twice that of OSFP. OSFP and OSFP-XD modules are not compatible.

Figure F-1 compares the OSFP and OSFP-XD modules and cages. Figure F-2 shows that the OSFP-XD cage is taller than that of the OSFP. Concomitantly, Figure F-3 shows that the OSFP-XD module is taller than the OSFP's, and that the connector mating paddle card design is different.

Mechanical keying prevents insertion of OSFP-XD modules into OSFP ports, and OSFP modules into OSFP-XD ports. These modules and ports combinations are incompatible. Despite the keying features, abuse and forced insertion of a module to wrong port can cause a mechanical damage to the port.

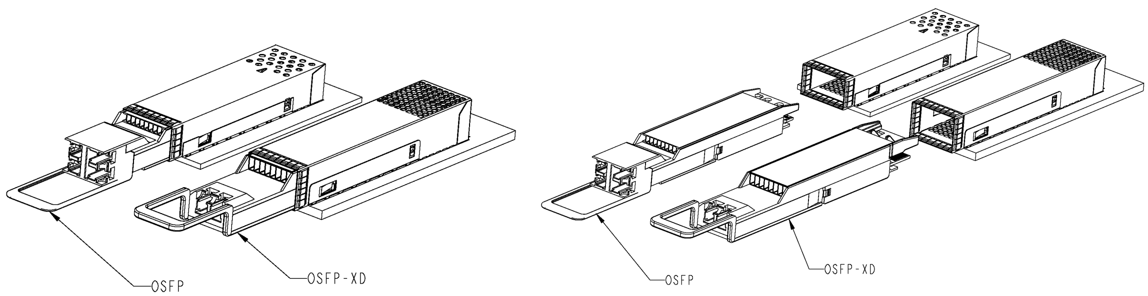


Figure F-1: OSFP and OSFP-XD, module and port

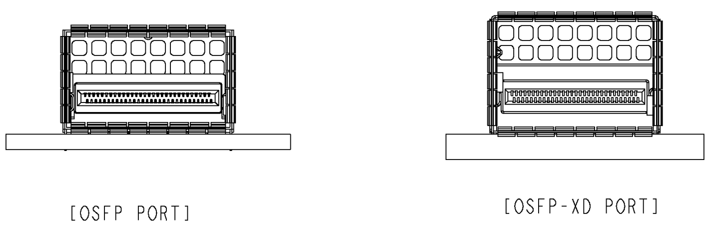


Figure F-2: OSFP and OSFP-XD, port front view

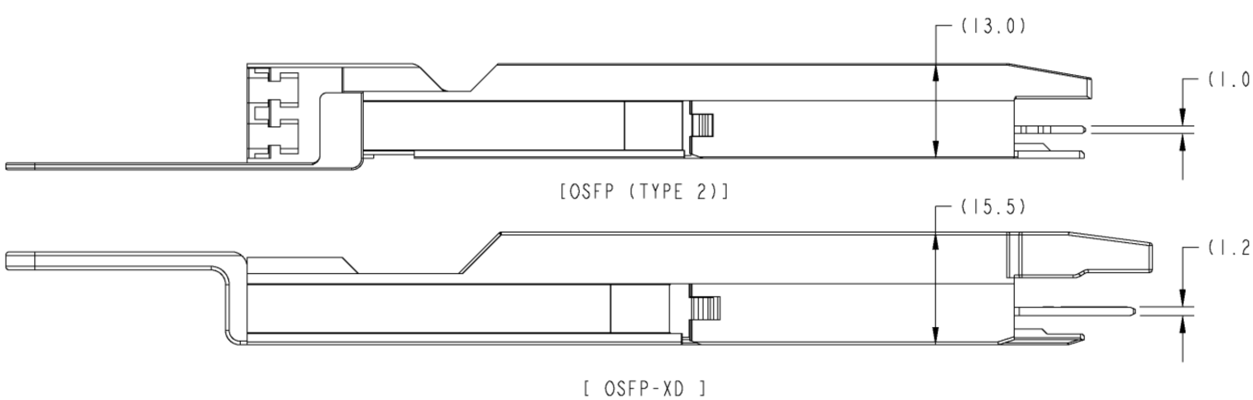


Figure F-3: OSFP and OSFP-XD, module side view

Appendix G. Thermal Monitoring for High Power Modules

** This section is adopted from the QSFP-DD Hardware specification Rev 7.1, Section 9.4.*

G.1 Thermal Characteristics for High Power Modules

In high power modules, the module implementer needs to ensure that the module meets all performance and reliability specifications and monitoring only the case temperature can result in overly conservative readings for the host equipment to use. Instead by monitoring all necessary internal component temperature sensors against their high temperature warning/alarm/shutdown limits, the module and host equipment can more accurately assess the component's margin to the various temperature limits that affect performance and reliability. To be compatible with the existing CMIS approach to report the case temperature Tcase, it is possible to convert these multiple sensor readings in such a way to provide the host equipment the ability to manage the system and module cooling without a change to CMIS software. The specific temperature sensors, including their values, thresholds and physical location are defined and known by the module implementor, and are not required to be advertised to the equipment supplier. Instead, the module's firmware shall process the monitored temperature data points against their limits, and provide the following to the equipment supplier via the management interface:

A high temperature monitor, which shall be a single monotonic increasing/decreasing value and be a consolidated leading indicator for all the module's defined sensor points against their high temperature thresholds (including warning, alarm, shutdown).

Module implementor's defined limits for the high temperature monitor values, including warning, alarm and shutdown thresholds are known. The least margin to these limits shall be advertised to the equipment supplier as the equivalent margin to the advertised case temperature limit via the management interface. The module's specified case temperature limits are recommended (but not required) to be consistent with temperature ranges classes defined in section 11.1.

The temperature monitors are expected to represent an accurate measurement of where the module operates relative to the temperature limits defined by the module supplier. The temperature monitors are not expected to represent a physical temperature at any specified location on or inside the module.

G.2 Example Procedure to Implement High Power Module Monitoring (Optional)

As an example, a procedure to calculate the high temperature case monitor temperature alarm threshold that is reported by the module in CMIS to the host is outlined below in a case where 3 temperature sensors are being monitored by the module firmware (laser, DSP, TIA):

Step I:

The module's case temperature monitored sensor reading (Tcase) should have internal module specified thresholds that are advertised via the management interface:

$Tcase_{warning\ threshold}$:Module case temperature warning threshold (for example 70 ºC)

$Tcase_{alarm\ threshold}$: Module case temperature alarm threshold (for example 75 ºC)

$Tcase_{shutdown\ threshold}$: Module case temperature shutdown threshold (for example 80 ºC)

Step II:

Including all monitored sensors, calculate the temperature margin for the leading indicator against the module's known internal warning, alarm and shutdown thresholds.

$margin_{warning} = min(Dt_{laser, warning}, Dt_{DSP,warning}, Dt_{tia,warning}, \ldots$ etc.)

$margin_{alarm} = min(Dt_{laser, alarm}, Dt_{DSP,alarm}, Dt_{tia,alarm}, \ldots$ etc.)

$margin_{shutdown} = min(Dt_{laser, shutdown}, Dt_{DSP,shutdown}, Dt_{tia,shutdown}, \ldots$ etc.)

Where $Dt_{A,B}$ is the temperature margin for sensor A against its high temperature B threshold (where B can be the warning, alarm or shutdown temperature threshold).

The calculation of the reported case temperature reading (Tcase) should be agnostic to how the module design defines the temperature thresholds of the monitored sensors, including temperature steps between warning, alarm and shutdown thresholds. One implementation that can accomplish this is outlined in step III below.

Step III:

Based on the margin with the smallest value greater or equal to zero, calculate the reported Tcase as below.

If $margin_{warning}$ is the smallest margin, greater or equal to 0:

$Tcase_{warning} = Tcase_{warning\ threshold} - margin_{warning}$

If $margin_{alarm}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{alarm threshold}} - margin_{\text{alarm}} * \frac{Tcase_{\text{alarm}} - Tcase_{\text{warning}}}{t_{\text{A,alarm}} - t_{\text{A,warning}}}$$

where $t_{\text{A,alarm}}$ and $t_{\text{A,warning}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.

If $margin_{shutdown}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{shutdown threshold}} - margin_{\text{shutdown}} * \frac{Tcase_{\text{shutdown}} - Tcase_{\text{alarm}}}{t_{\text{A,shutdown}} - t_{\text{A,alarm}}}$$

where $t_{\text{A,shutdown}}$ and $t_{\text{A,alarm}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.