OSFP MSA

Specification for

OSFP-XD, OCTAL SMALL FORM FACTOR eXtra Dense PLUGGABLE MODULE

Rev 1.1

September 12th, 2024

Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, mechanical and thermal requirements of the OSFP-XD Module, connector and cage systems. The OSFP-XD Management interface is described in a separate document, Common Management Interface Specification (CMIS).

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Revision History:

Rev 1.1	9/12/2024	In section 3, the module bottom lead-in chamfer is updated to 17.5° (Figure 3-7); module back vent hole dimensions are updated (Figure 3-12); module paddle card power pad length is updated (Figure 3-37) - leading pre-wipe pad became optional, and the pre-wipe pads between the rows of power/ground is also optional. In section 4, minimum cage latching flap length is added (7.0mm); connector max width was increased to 22.48mm; footprint of the connector is changed to use plated pad as seating plane. In section 6, maximum module insertion force is increased by 10N (50N max). In section 8, OSFP-XD-RHS bottom lip is thicken from 1.0mm to 1.5mm; RHS module back top thickness specification is updated to 0.90mm minimum. Section 12.4 is updated to clarify the optical connector lane assignments. Appendix A, B and C are added.
Rev 1.0	3/17/2023	Initial Release

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1 Scope

The OSFP-XD specification defines:

- The OSFP-XD module mechanical form factor, including latching mechanism and heatsink;
- Host cage together with the mating connector;
- Electrical interface, including pin-out, data, control, power and ground signals;
- Mechanical interface, including package outline, front panel and printed circuit board (PCB) layout requirements;
- Thermal requirements and limitations, including heat sink design and airflow;
- Electrostatic discharge (ESD) requirements;
- The module management interface as contained in the Common Management Interface Specification (CMIS).

2 References

- IEC 61754-7-1:2014: Fibre optic interconnecting devices and passive components – Fibre optic connector interfaces – Part 701: Type MPO connector family – One fibre row
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- UM10204, I^2C-bus specification and user manual, Rev 7 – 1 OCT 2021
- MIPI $I3C^{SM}$ HCI^{SM} v1.2, MIPI Alliance, April 2023
- SFF-8679: Specification for QSFP+ 4X Base Electrical Specification, Rev 1.8 October 4, 2018
- SFF-8024: Specification for SFF Module Management Reference Code Tables, Rev 4.12, July 9, 2024
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
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- IEEE802.3bs: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation
- IEEE802.3cd: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation
- IEEE802.3bj: Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables
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- IEEE802.3ck: Amendment 4: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling

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- Senko SN®-MT connector, https://www.senko.com/product/sn-mt-connector/
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- OIF-CEI-05.1, Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps, and 112G+ bps I/O, 2022, Optical Internetworking Forum, https://www.oiforum.com/wp-content/uploads/OIF-CEI-5.1.pdf
- Press Release, AirMT™ series Non-contact MT Technology, https://global-sei.com/company/press/2019/09/prs072.html
- 3M™ Expanded Beam Optical Connector (EBO), https://www.3m.com/3M/en_US/data-center-us/applications/interconnect-optical/
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- USConec MMC connector, https://www.usconec.com/featured-products/mmc-connector
- Specification for OSFP Octal Small Form Factor Pluggable Module, Rev 5.1, www.osfpmsa.org

3 OSFP-XD Module Mechanical Specification

3.1 Overview

A typical OSFP-XD module is shown in Figure 3-1. Connector and cable variations not shown here are allowed.

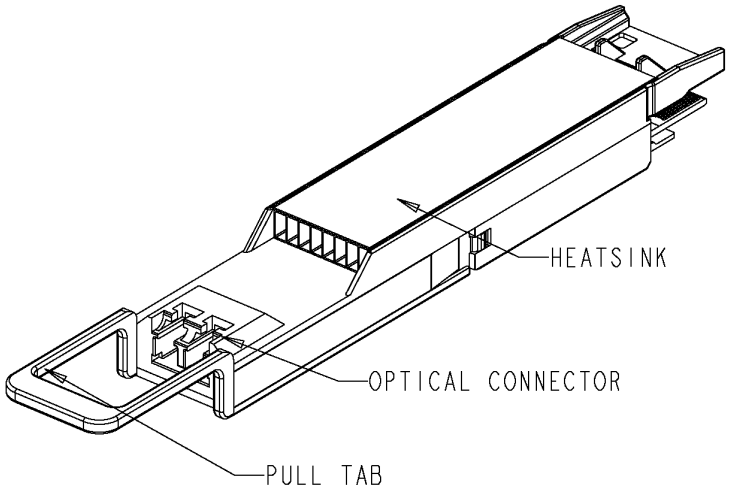


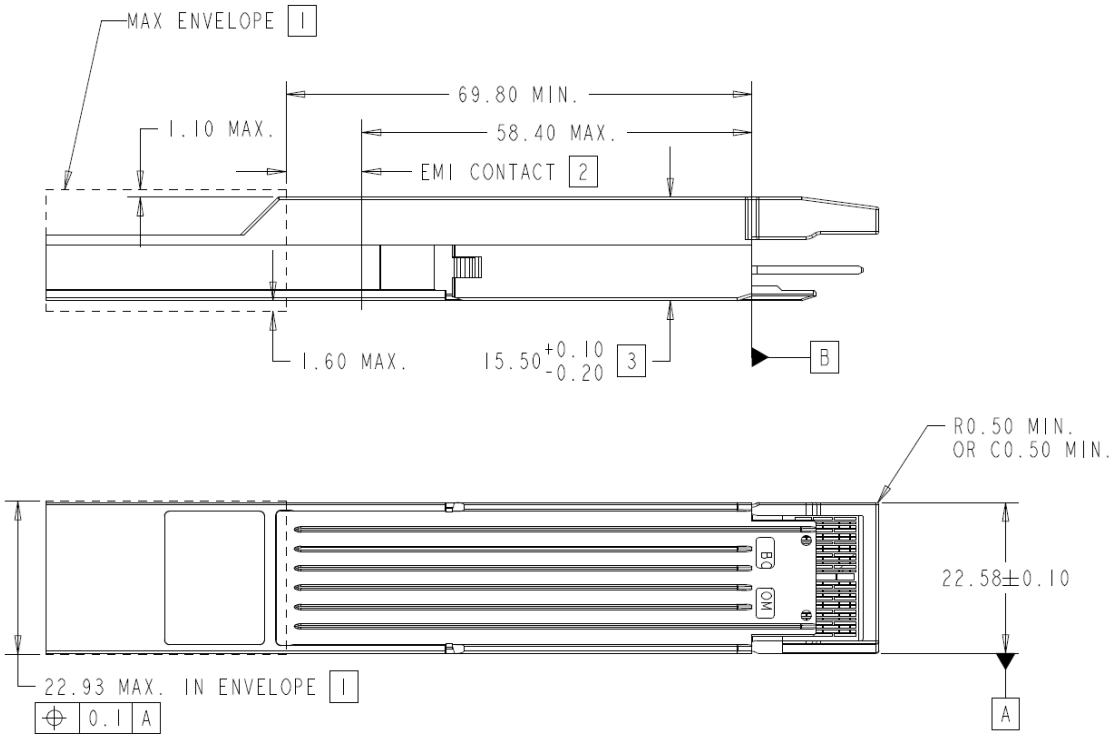
Figure 3-1: OSFP-XD module with a LC connector

In the module mechanical drawings included throughout this specification, the datum as defined in Table 3-1 shall apply.

Table 3-1: Descriptions of the module mechanical datum

Designator	Description	Figure
A	Width of the module	Figure 3-2
B	Forward stop of the module	Figure 3-2; also see Figure 3-11
C	Bottom surface of the module	Figure 3-6
D	Width of module printed circuit board	Figure 3-37
E	Signal pad leading edge of the module printed circuit board	Figure 3-37
F	Top surface of the module pc board	Figure 3-37

Figure 3-2 shows the dimensions of the OSFP-XD module. Note that the module is shown with a typical latch release mechanism without a pull tab. Alternate latch release mechanisms are allowed. All dimensions in this specification are in millimeters (mm) unless otherwise noted.



NOTES:

1. FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.6mm MAX FROM THE BOTTOM OF THE MODULE, 1.1mm MAX FROM TOP AND CAN HAVE UP TO 22.93mm WIDTH WHERE SHOWN.
2. INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
3. APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

Figure 3-2: OSFP-XD overall dimensions

For the length of the module, there can be Type 1 (standard) and Type 2 (with extra length) modules as shown in the Figure 3-3.

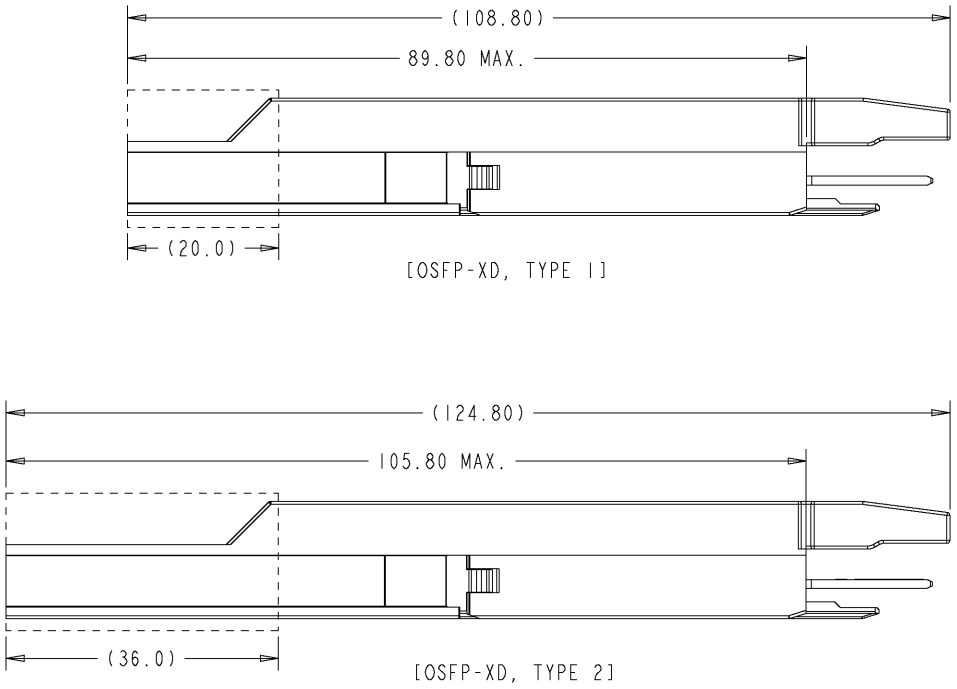


Figure 3-3: OSFP-XD type 1 and 2 (module length)

Module may have pull tab to release the latch behind the cable; the recommended length of the pull tab with respect to the module positive stop feature is shown at Figure 3-4, which applies both to the type 1 and type 2 module. The pull tab shown in the figure is reference only and the shape may differ.

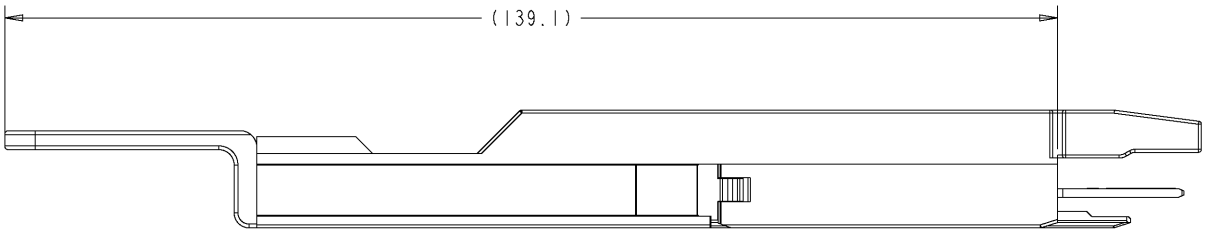


Figure 3-4: OSFP-XD Pull tab length

Figure 3-5 shows the radius on the corner of the module, to prevent the damage on the internal EMI fingers on the cage.

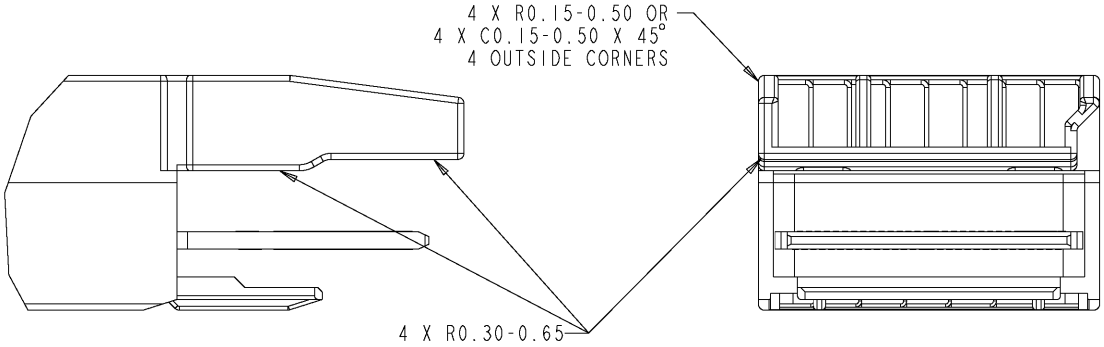


Figure 3-5: OSFP-XD corner radius

3.2 OSFP-XD, Back of the Module

To mate with an electrical connector located in the cage, an OSFP-XD module shall have a protruded printed circuit board (PCB) with contact pads. A structure in the back of the module serves as a guard to protect the PCB and gives lead-in when the module is inserted to the cage. Figure 3-6 through Figure 3-14 show the dimensional requirements of the back of the module, including the shape of the structure, connector mating area, forward stop, ventilation holes and location of the signal pads.

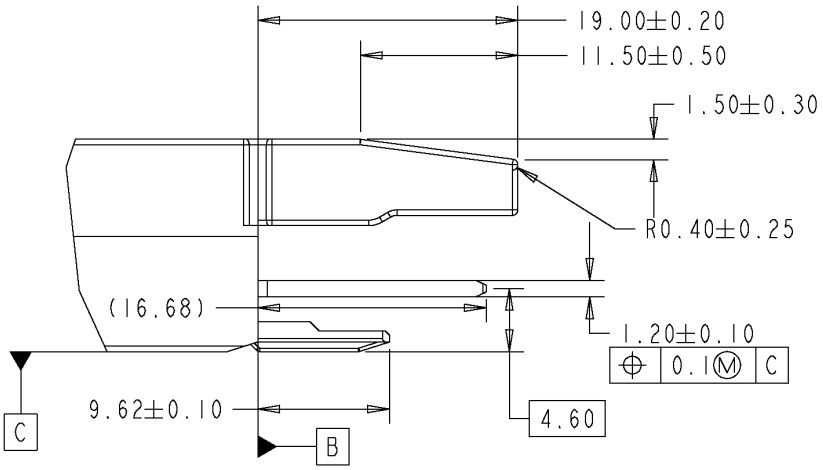


Figure 3-6: OSFP-XD back, in a side view

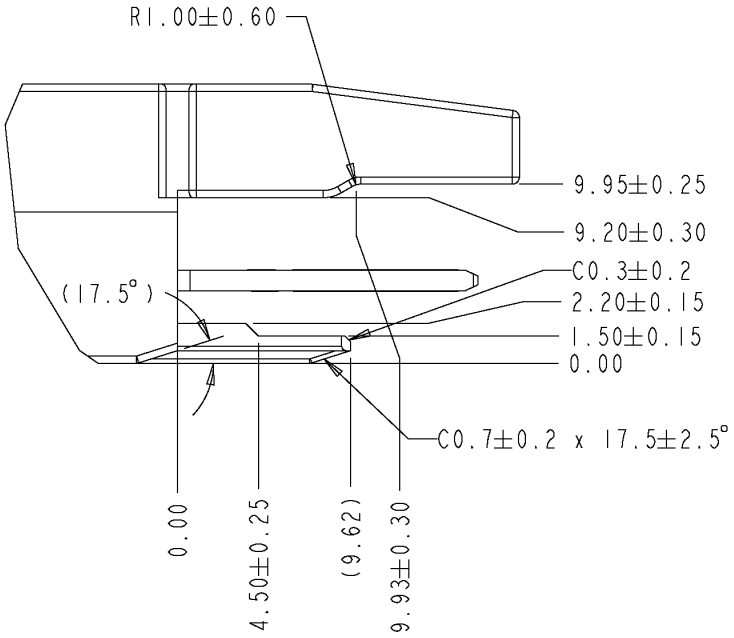


Figure 3-7: OSFP-XD, structure shape

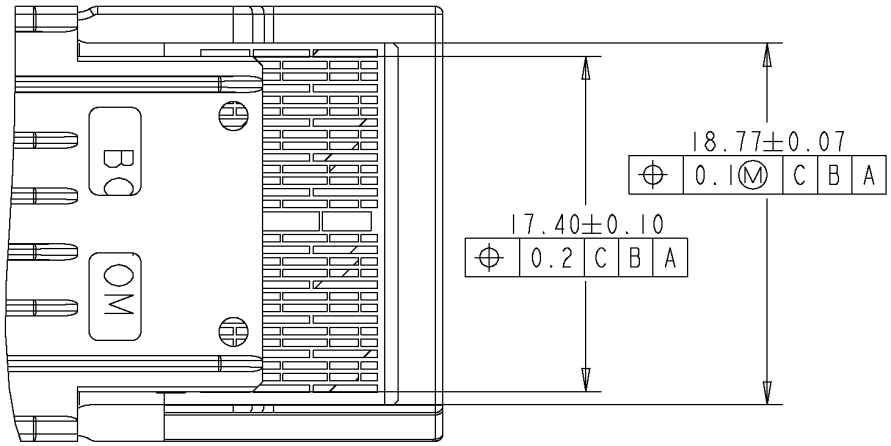


Figure 3-8: OSFP-XD, back, in the bottom view

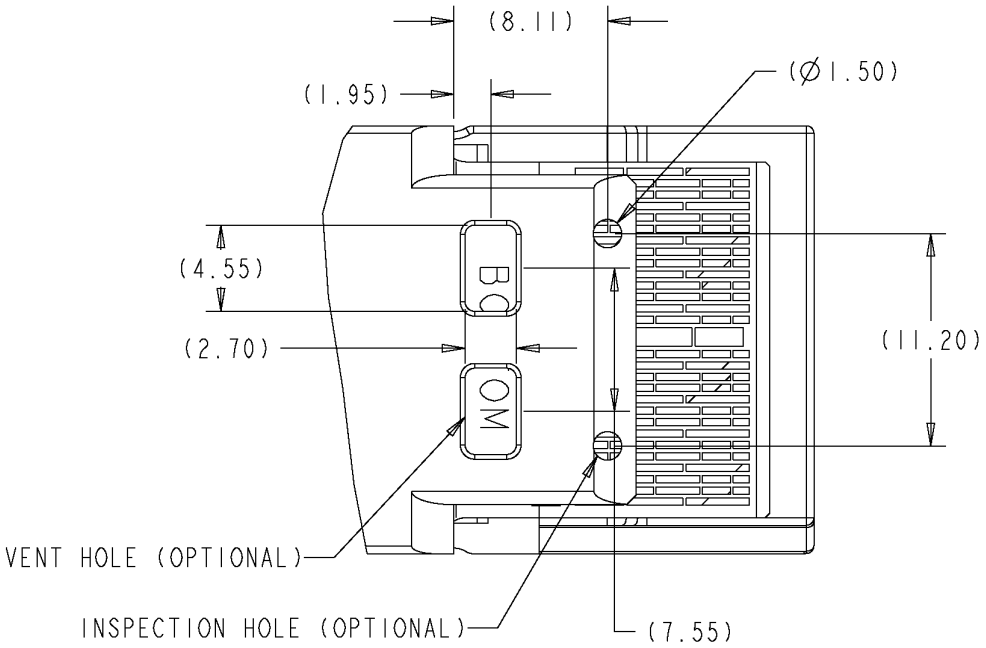


Figure 3-9: OSFP-XD, optional signal pad inspection holes

In the bottom back of the module, there can be optional ventilation holes and pad location inspection holes as in the Figure 3-8 and Figure 3-9.

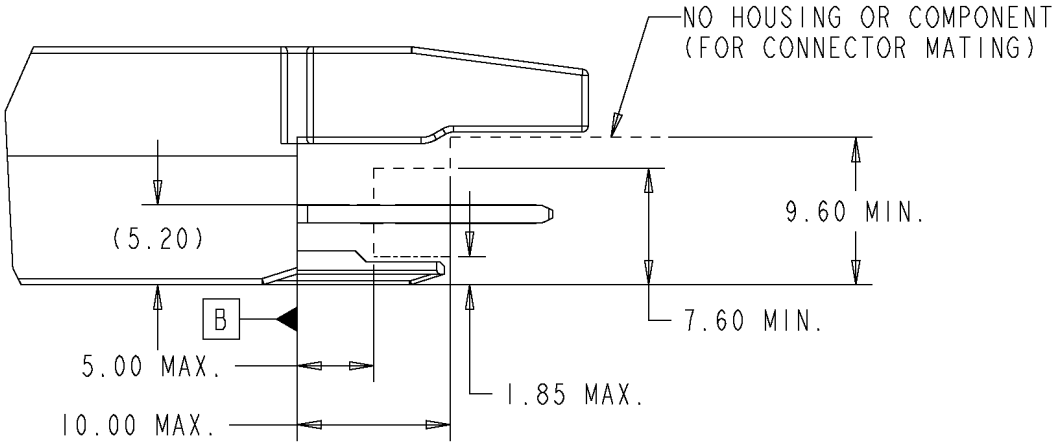


Figure 3-10: OSFP-XD, no component area

Figure 3-11 shows the location of the forward stop, consisting of the left and right vertical side walls of the bottom case of the module, which interact with features in the connector cage to stop the module when it is fully inserted.

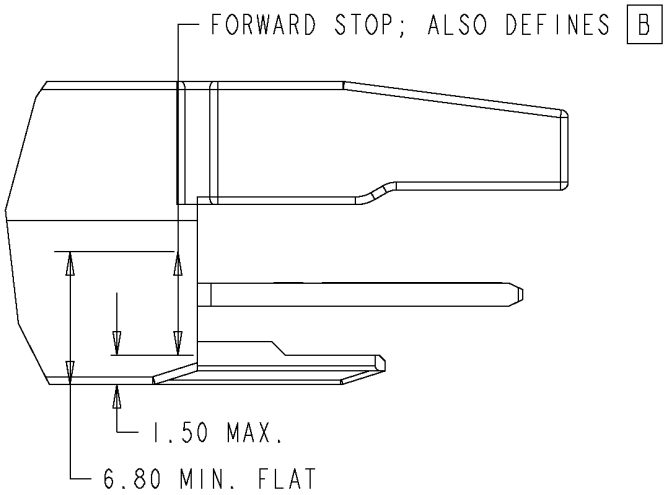


Figure 3-11: OSFP-XD, location of the forward stop

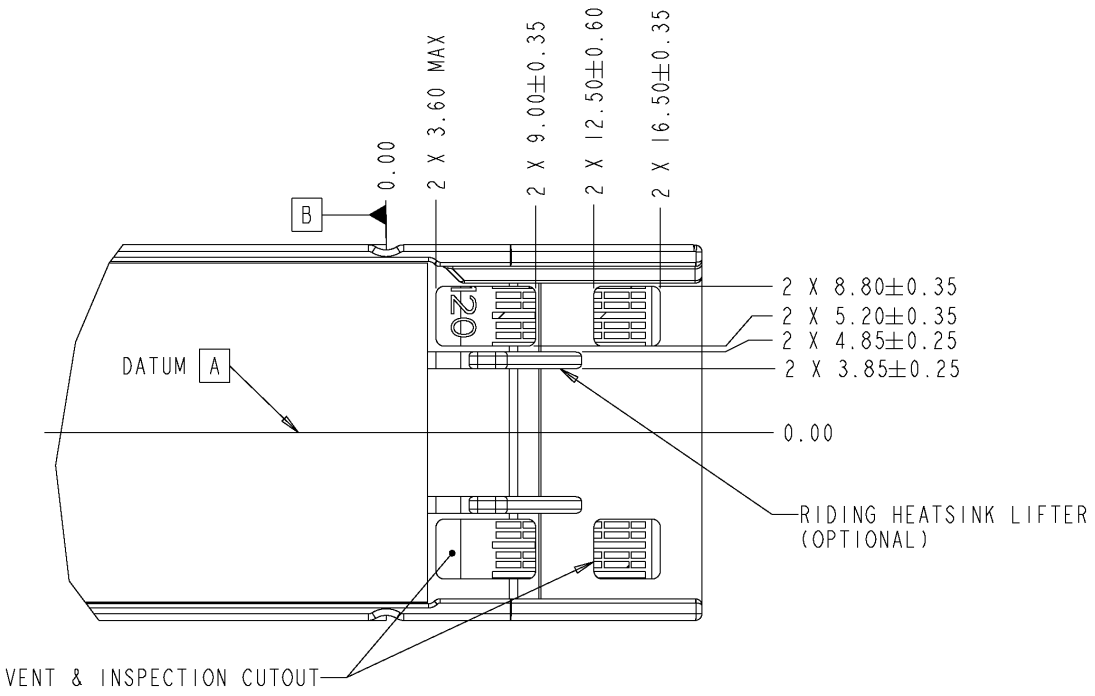


Figure 3-12: OSFP-XD, dimension for ventilation holes

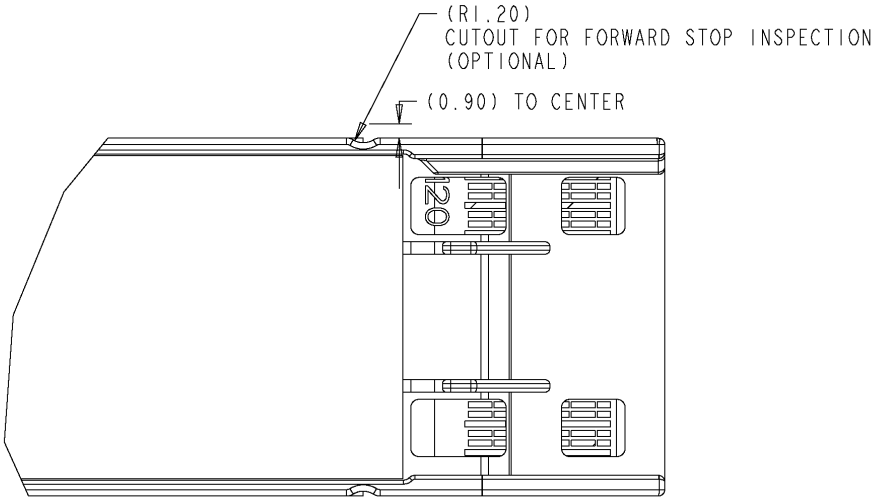


Figure 3-13: OSFP-XD, optional stop inspection groove cutout

Figure 3-12 shows the cutout on the shell, which can be used for the inspection of the pad location. Also, those holes can serve as extra ventilation holes if the module have airflow channel at the bottom side of the module.

Figure 3-13 shows optional grooves on the module to inspect the location of the forward stop; such feature should be designed as in the figure, so that it does not damage the internal EMI fingers of the cage.

Figure 3-14 shows the location of the leading edge of the signal pads with respect to the module positive stops.

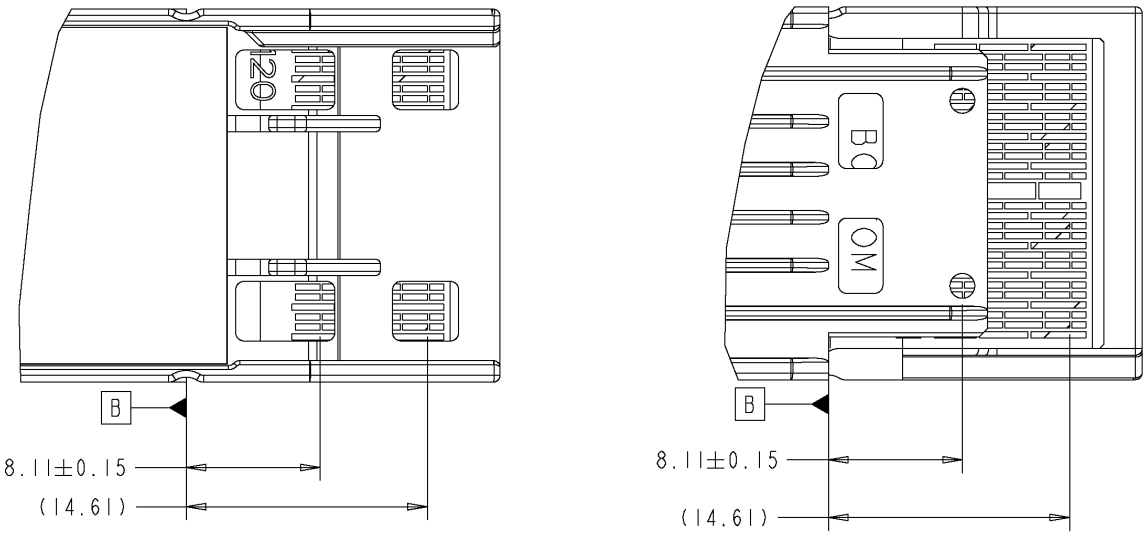


Figure 3-14: Signal pad location to module (left: top view, right: bottom view)

3.3 Keepout for Keying

OSFP-XD modules have a keepout space on the back, which is used for the keying. There shall be matching feature in the cage. This keying feature will protect the OSFP-XD connector when a legacy OSFP module is inserted to the OSFP-XD cage. Figure 3-15 shows the length of the keying feature. Figure *3-16* shows the keying keepout space. The keying keepout shall be only one side of the module, as shown in the Figure *3-16*.

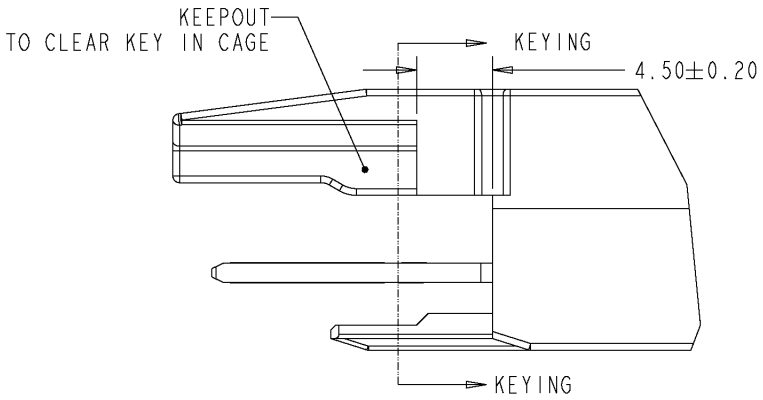


Figure 3-15: OSFP-XD, keying feature length

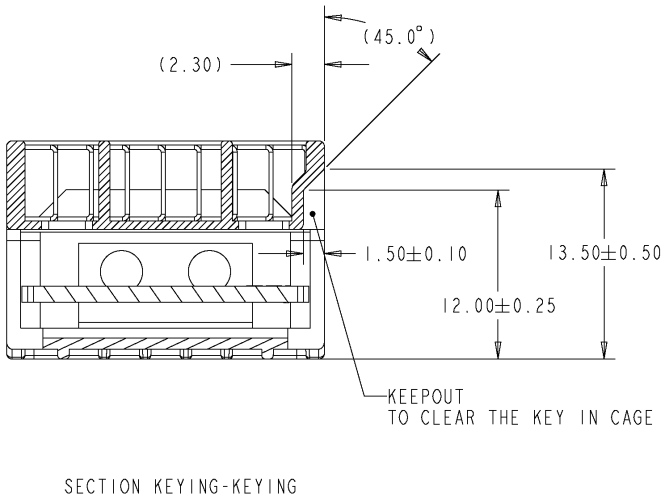


Figure 3-16*: OSFP-XD, keying feature height (section view)*

3.4 Heat Sink

To dissipate heat from the module, the module will provide the airflow passage. The airflow passage can have heatsink, and also will block the EMI radiation from or into the host system. And it should not damage the internal EMI finger of the cage, and may work with optional riding heatsink on the cage.

There can be various design of the heatsink for the top side of the module, as shown in the Figure 3-17.

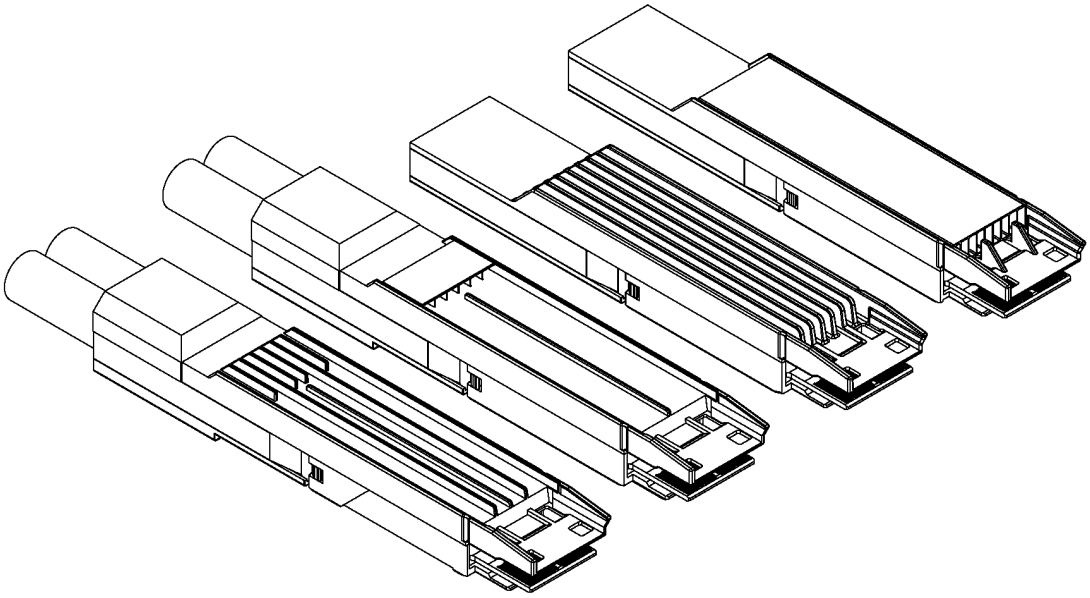


Figure 3-17: OSFP-XD, various heatsink shape

As the top heatsink design can be varied, there can be different module bottom side design. In this section, the top heatsink design will be depicted. See Section 3.6 for the details of the bottom side of the module. The designs shown in this section, although they are reference designs, should be able to meet the airflow requirement in the Section 7.3.

Figure 3-18 shows a zipper fin heatsink on the top of the module. In this case, the module have airflow channel with the EMI clip on the bottom for extra airflow from the bottom side.

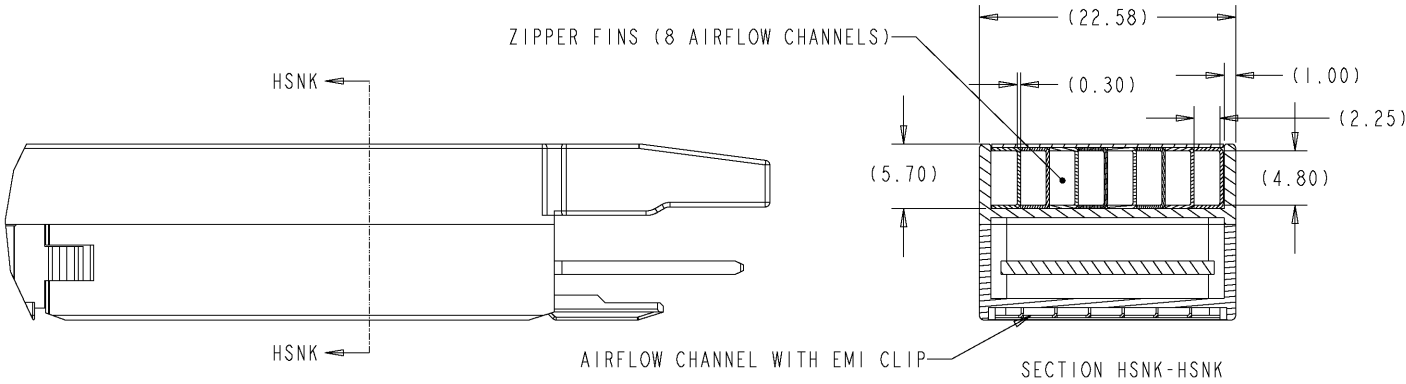


Figure 3-18: Heatsink, Zipper fin

Figure 3-19 shows an extruded aluminum heatsink on the top of the module.

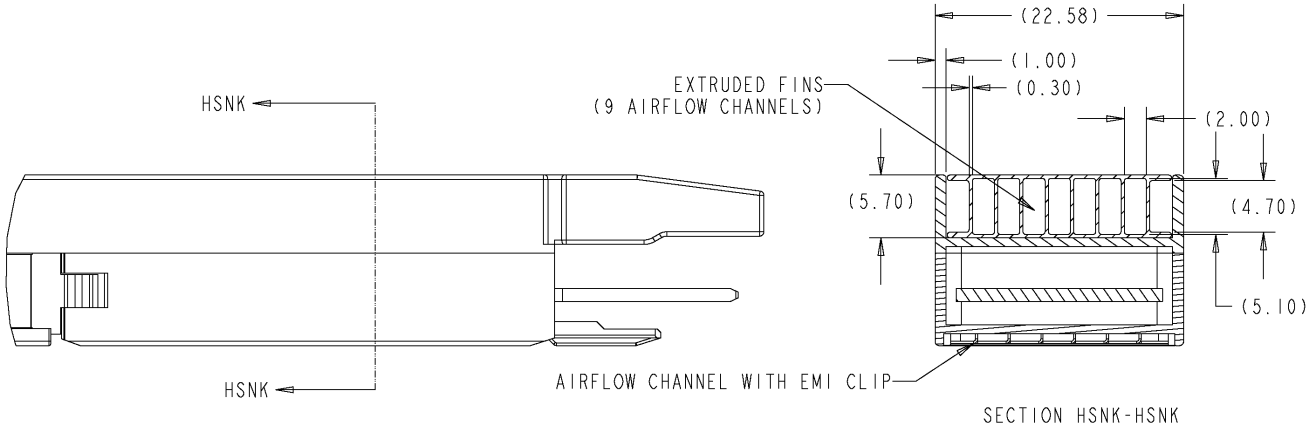


Figure 3-19: Heatsink, Aluminum Extrusion

The OSFP-XD may be used for a port with riding heatsink. To enable the smooth insertion of the module with the riding heatsink, the leading edge of the heatsink should not have sharp edge as shown in the Figure 3-20. Same figure showed optional heatsink lifter to further help the insertion.

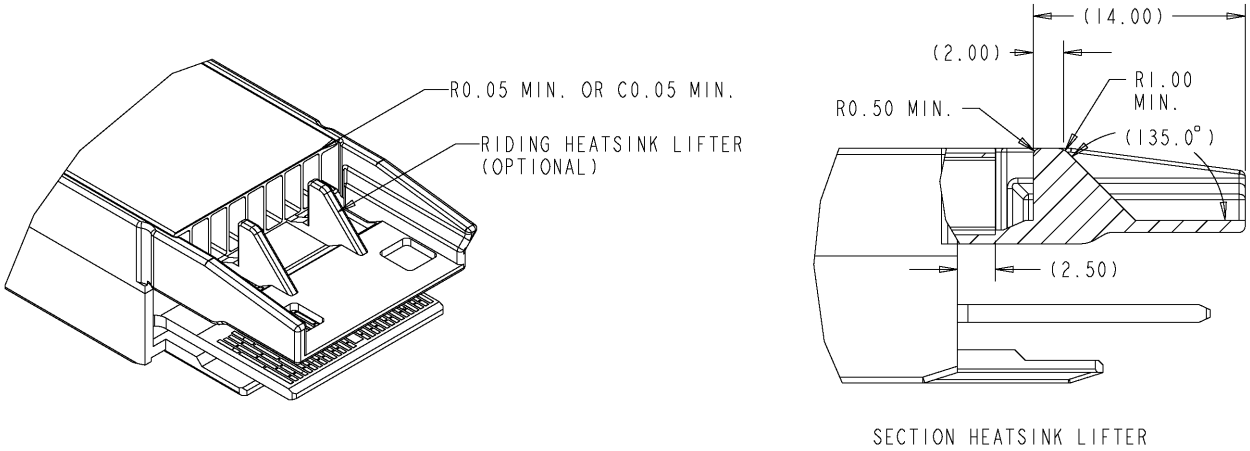


Figure 3-20: Heatsink lifter (Right: sectional view)

Figure 3-21 shows the shell which have integrated heatsink fin (open top). For the open top, the pitch of the fins should match with the Figure 3-21 and Figure 3-22 to ensure proper EMI finger contact and also to prevent the EMI finger damage.

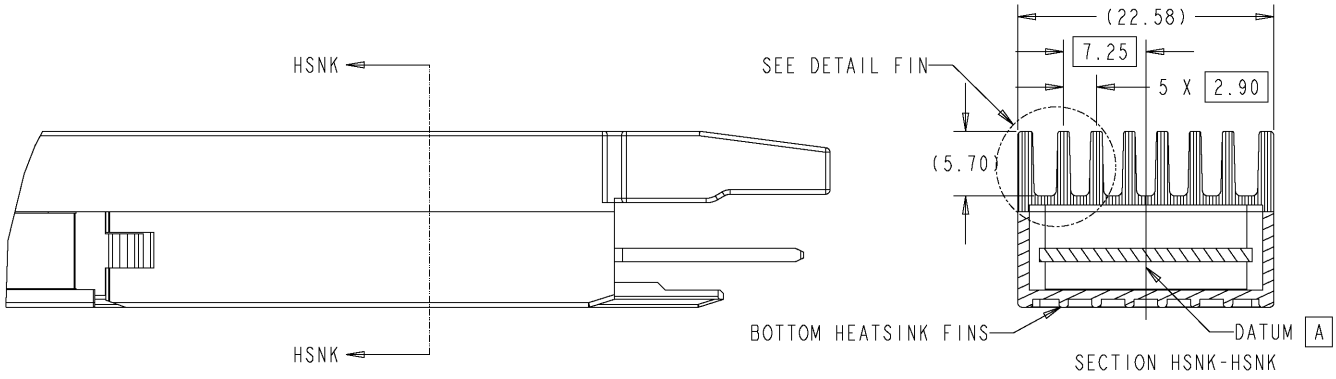


Figure 3-21: Heatsink, Open Top

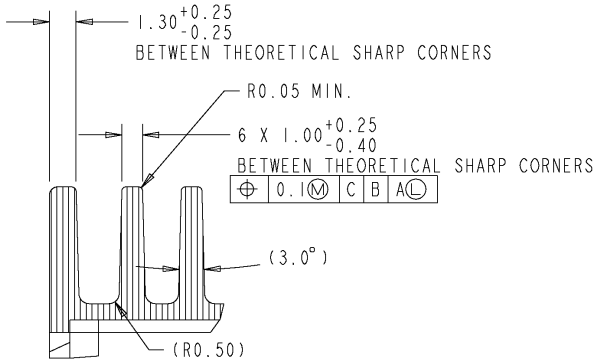


Figure 3-22: Heat sink, Open top, Detail Fin

For open top, the leading edge should not have sharp edges but have rounds as in the Figure 3-23.

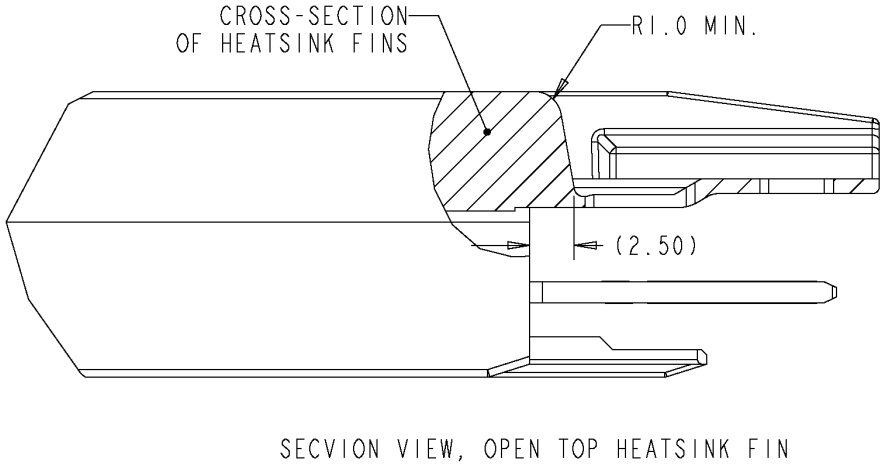


Figure 3-23: Heat sink, Open top, Leading edge

In cases where the extra module internal volume is necessary, a smaller airflow channel is allowed if the module is dissipating power less than 20W. Figure 3-24 shows a reference design for the passive copper cable, where the module have thin zipper fin used for the EMI blockage only and a short fin in the middle. As the fin in the middle does not match with the heatsink pitch in the Figure 3-21, the fin should be short as shown and avoid contact with the cage EMI fingers during the insertion and removal of the module. The module shown here does not have any airflow channel on the bottom.

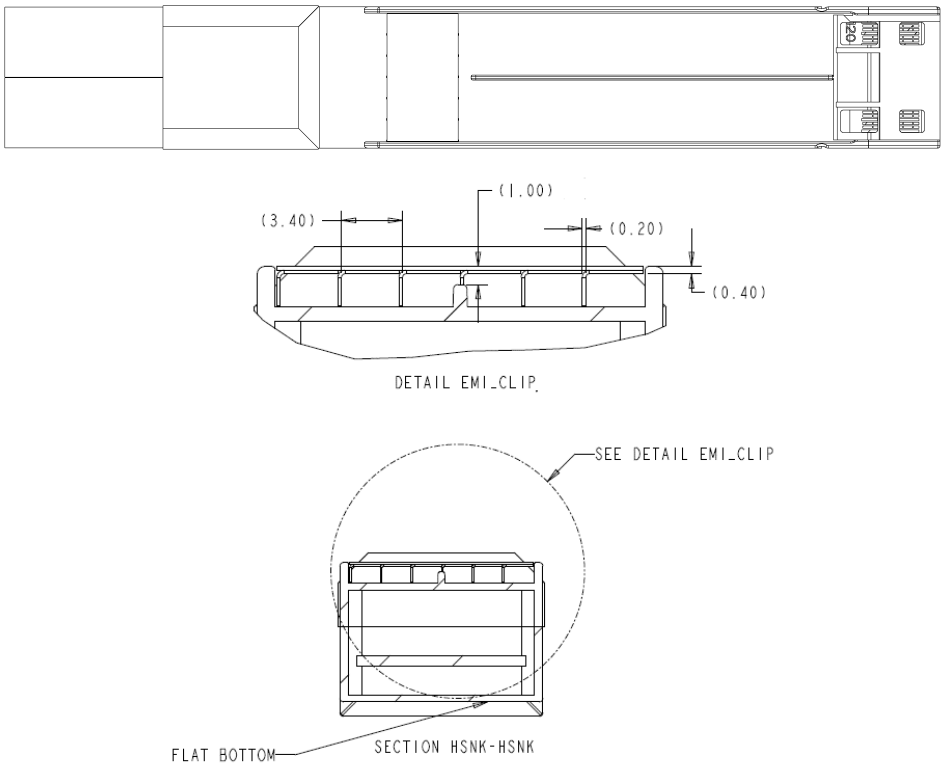


Figure 3-24: Heat sink, EMI clip airflow channel

Figure 3-25 shows another alternative design, where the integrated open top heatsink is on the top side. The height of the heatsink is shorter than shown in the Figure 3-21. And some of the fins are shorter, so that it works mainly to make ground contact with EMI fingers on the cage only. In this example, the module has recess on the bottom to pass extra air to the host system.

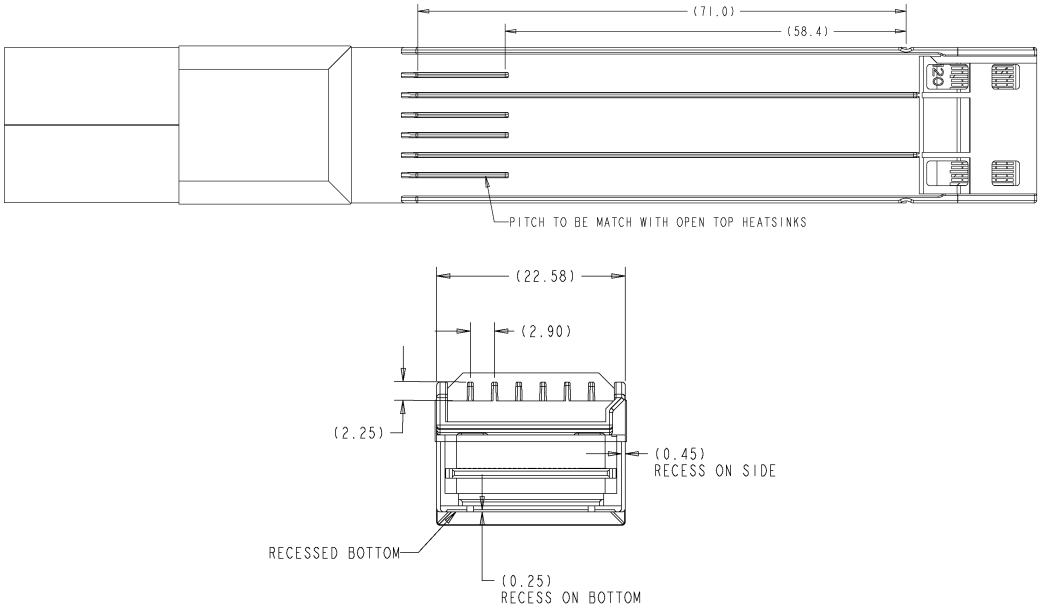


Figure 3-25: Heat sink, Open top, short

3.5 Surface Requirement for the Flat Top

OSFP-XD module may be plugged into the port which has a riding heatsink, and a properly designed module can have extra thermal benefit from the riding heatsink. For the module with flat top, top surface will be thermally conductive so it can work with an extra riding heatsink. Figure 3-26 shows the thermal conductive area for the top of the module. This area should have surface flatness and roughness as in Table 3-2. Section 4.6 shows the optional riding heatsink on the cage.

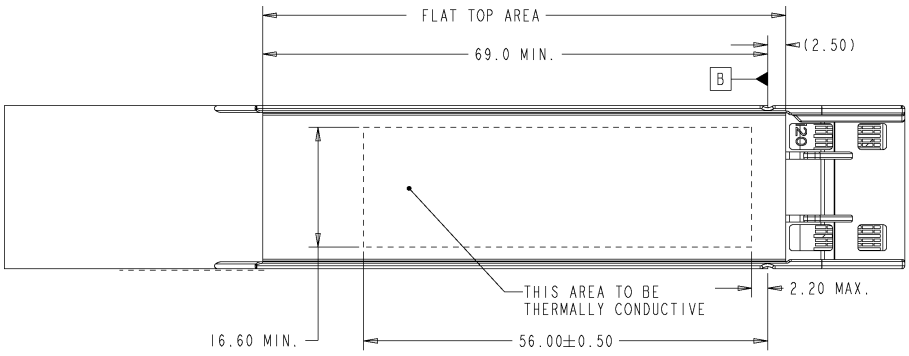


Figure 3-26: OSFP-XD, thermal conductive area

Table 3-2: Surface flatness and roughness for the thermally conductive area

Module Power (Max.)	Surface Flatness	Surface Roughness
N/A	0.12mm or better	Ra 1.6μm or better
Recommended for module with more than 20W (Optional)	0.075mm or better	Ra 0.8μm or better

3.6 Bottom of the Module

In the previous section, various top heatsink designs are provided as reference, and there were various bottom designs of the modules were used. In this section, example bottom designs are depicted as in the Figure 3-27. Different top and bottom shape can be combined to achieve the best thermal performance; but module designer must consider the EMI grounding requirement as in the Figure 3-2, open top pitch design as in Figure 3-21 and airflow impedance requirement as in Figure 7-1. Note that in all cases, bottom should have no sharp catching edges which can damage the cage internal EMI fingers.

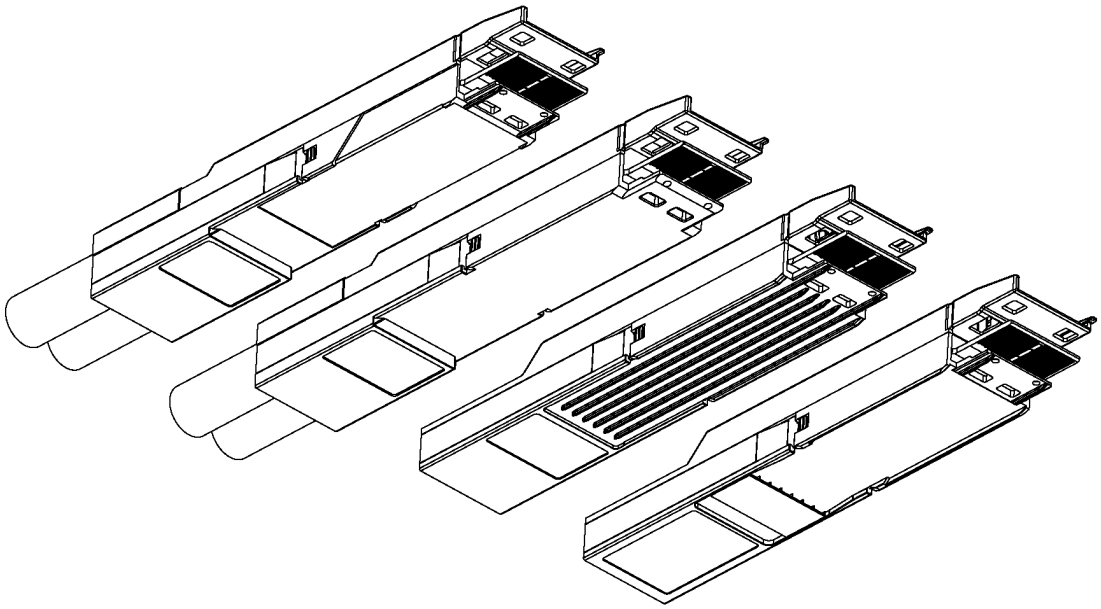


Figure 3-27: OSFP-XD, various bottom shape

Figure 3-28 shows the flat bottom, where there is no airflow channel to the bottom of the module.

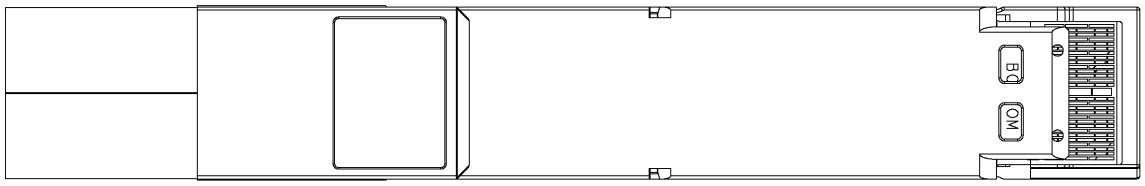


Figure 3-28: OSFP-XD, Flat bottom

Figure 3-29 shows a module with bottom heatsink fins. Short integrated heatsink fins are placed with a pitch as already defined in the Figure 3-21. This will provide extra airflow and cooling to the module, compared to the flat bottom.

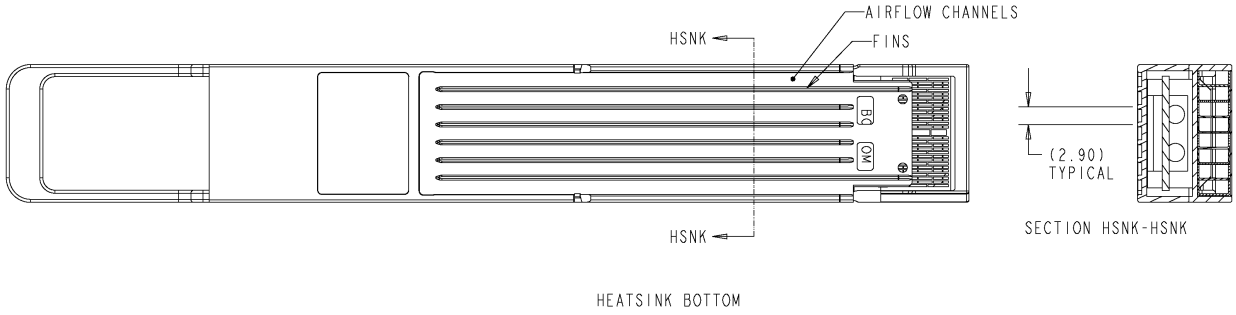


Figure 3-29: OSFP-XD, Bottom heatsink fins

Figure 3-30 shows a wider airflow channel, without extra heatsink fins, but a zipper fin features to provide the EMI shielding to the module. This design provides extra airflow thorough the bottom of the module.

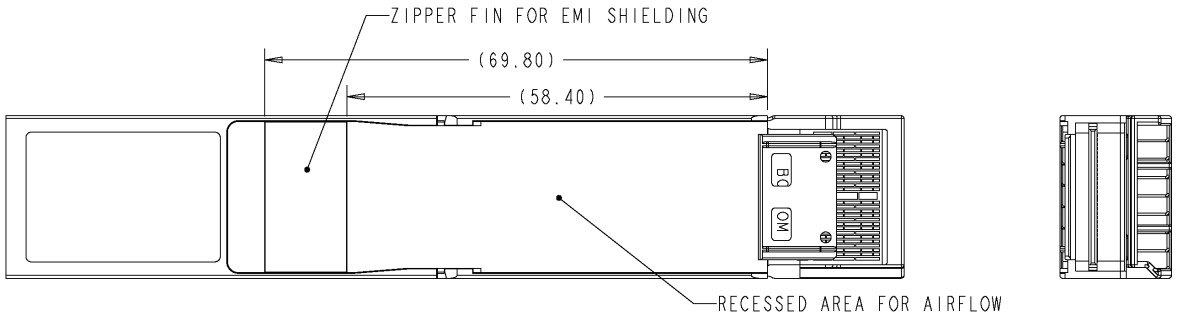


Figure 3-30: OSFP-XD, EMI clip bottom

Figure 3-31 shows recessed bottom of the module; the module have airflow channel on the bottom. It does not extend to the outside of the cage, thus airflow to this channel is coming from the vent on the bottom of the cage. Also, there is extra recessed area to both side of the module, to allow more airflow. The vent on the bottom of the cage is shown in the section 4.4 and section 4.8.

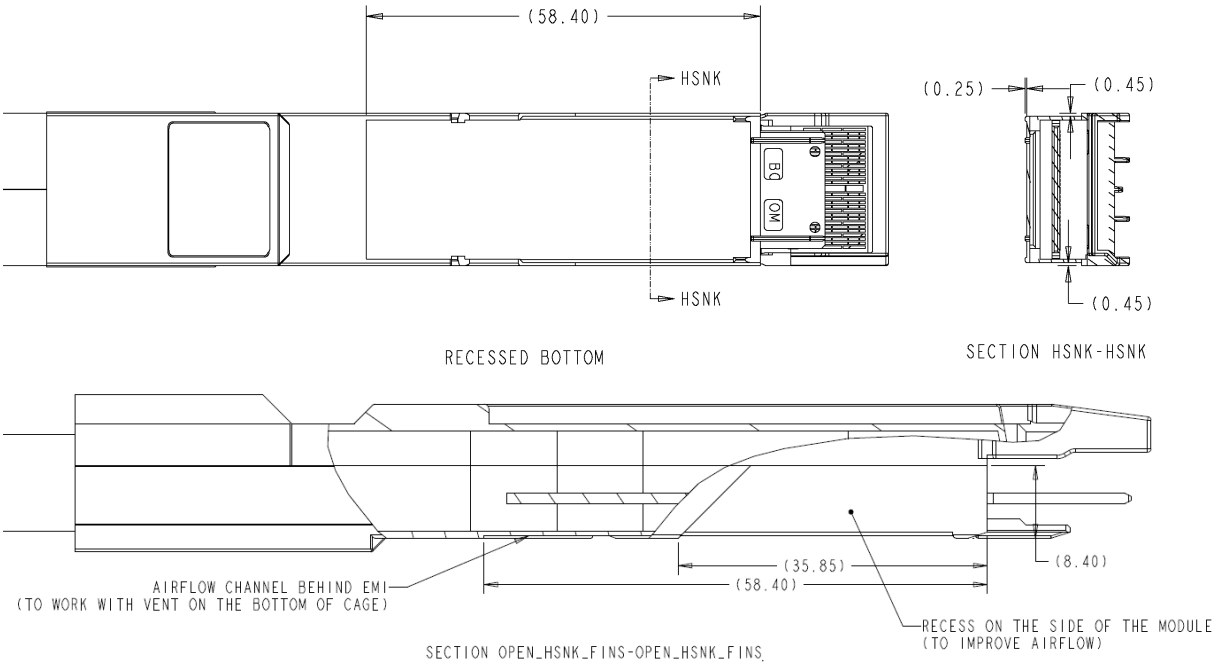


Figure 3-31: OSFP-XD, recessed bottom

Figure 3-32 shows details of the bottom side of the back of the module. For the module which does not have any airflow channel on the bottom side, bottom side of the back of the module can be solid as of Figure 3-33.

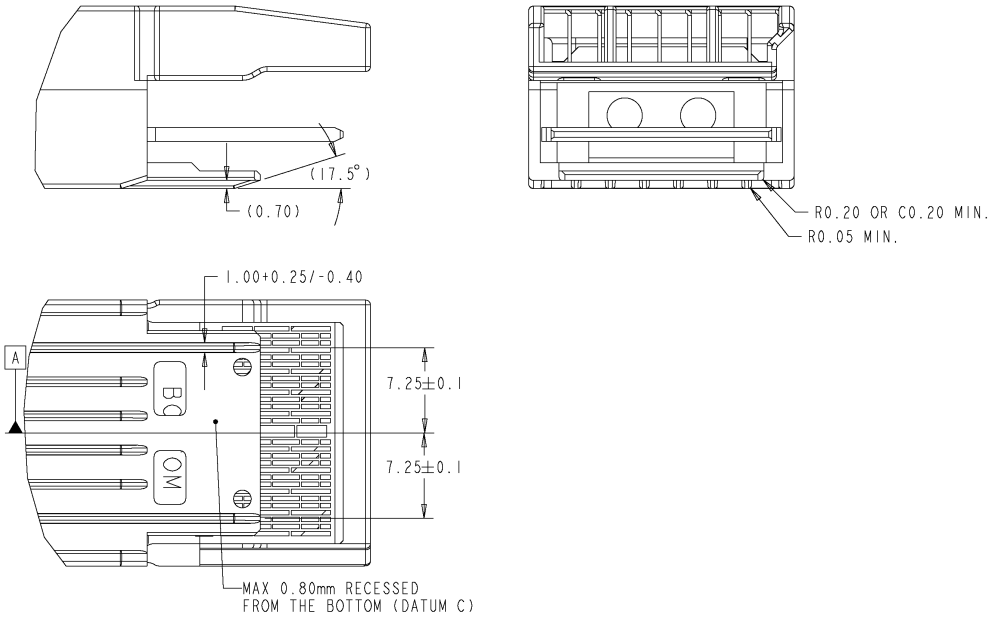


Figure 3-32: OSFP-XD, Ribbed bottom back

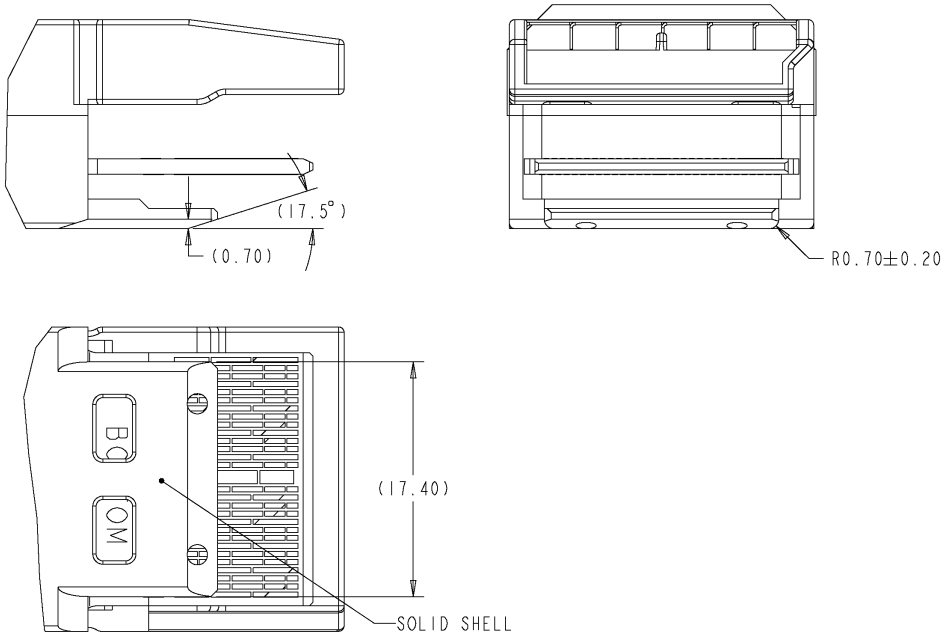


Figure 3-33: OSFP-XD, Solid bottom back

3.7 Label

Module shall have a label to identify. The location of the label is preferred to be at the bottom, and the front of the module which sticks outside of the cage as shown in the Figure 3-34; or, if the space is available, then a bigger size of the label as of Figure 3-35 can be placed.

Figure 3-34: OSFP-XD, preferred label location

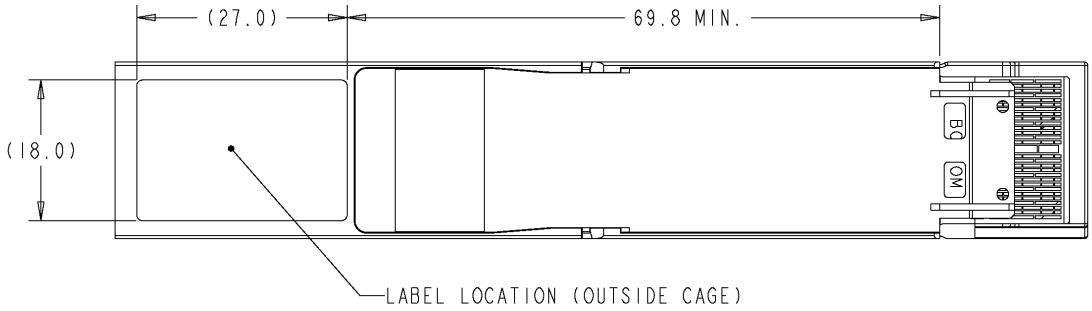


Figure 3-35: OSFP-XD, Alternative label size

If required, the label can be placed in a different location as in the Figure 3-36. When the label is placed inside the cage, the label should be placed in the recessed area not to snag on the EMI finger of the cage.

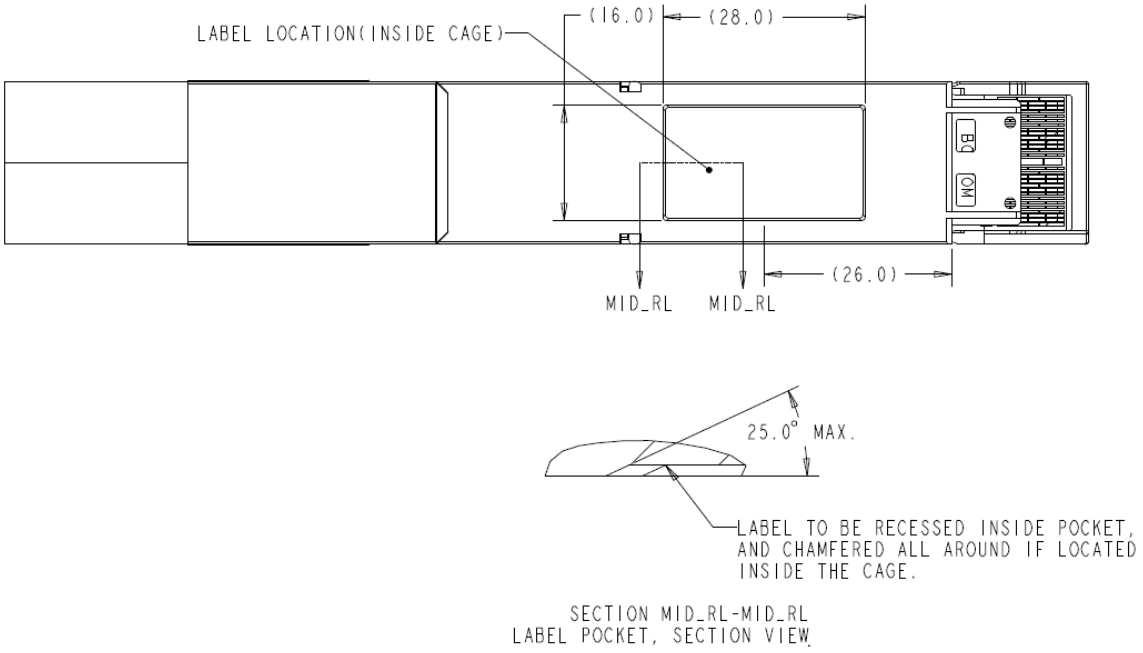


Figure 3-36: OSFP-XD, optional label location

3.8 Card-edge Design (Module Electrical Interface)

The OSFP-XD module contains a PCB with contact pads (i.e. module PC board; paddle card) that mate with a connector as specified in Section 4.12 of this document. Critical dimensions for the contact pads are shown in Figure 3-37 through Figure 3-39. The contacts are made in dual row, which mates with dual rows of the connector.

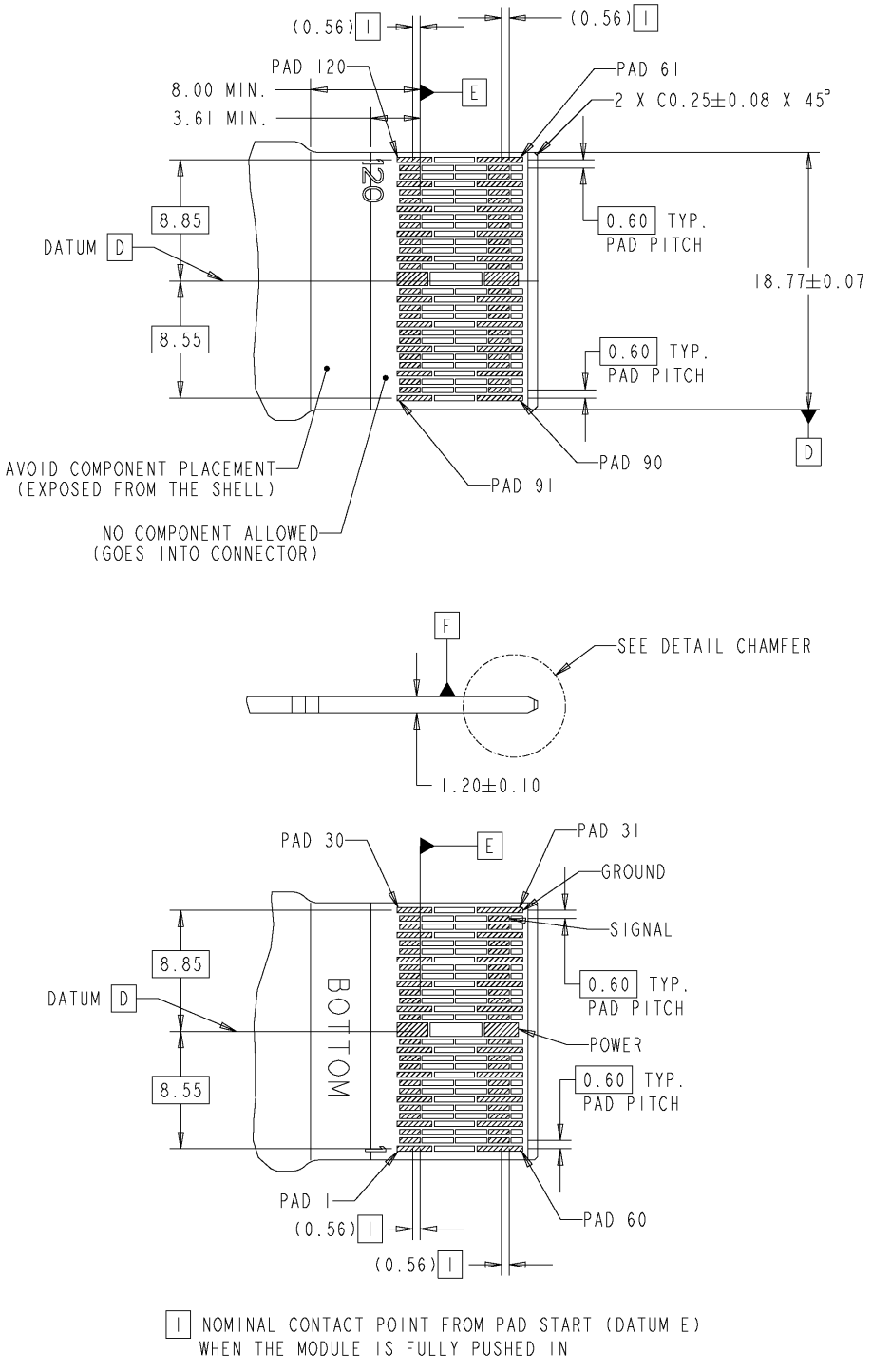


Figure 3-37: OSFP-XD module pc board (card-edge)

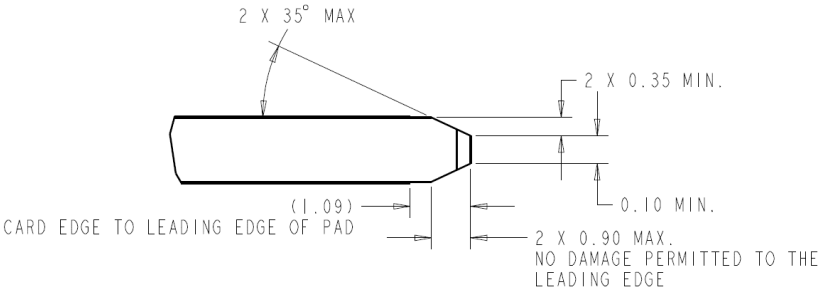


Figure 3-38: OSFP-XD card-edge, detail chamfer (lead-in chamfer)

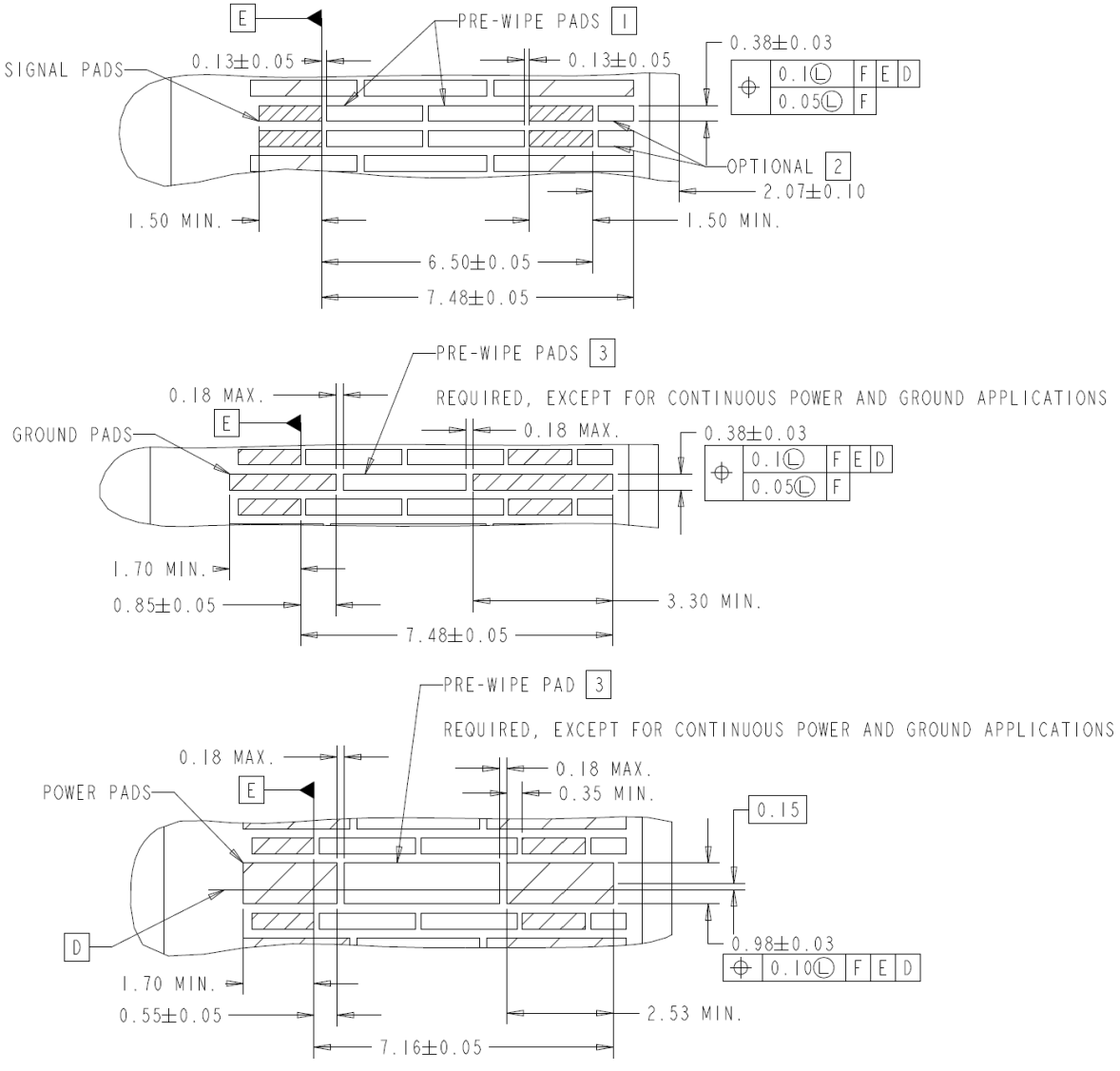


Figure 3-39: OSFP-XD card-edge, details of the pads

3.9 Contact Pad Plating Requirements

The contact pad plating shall meet the durability requirements of Section 6.1 and Section 6.2. The recommended plating specification is 0.762 µm minimum gold over 3.81 µm minimum nickel. Other plating systems are allowed provided they meet or exceed the requirements of Section 6.1 and 6.2.

3.10 Module Latch Feature

For latching, the module shall have latching pockets and a latch release mechanism at both sides as shown in Figure 3-40 to Figure 3-43. Dimensional details of the cage flap can be found in Figure 4-23 and Figure 4-24 .

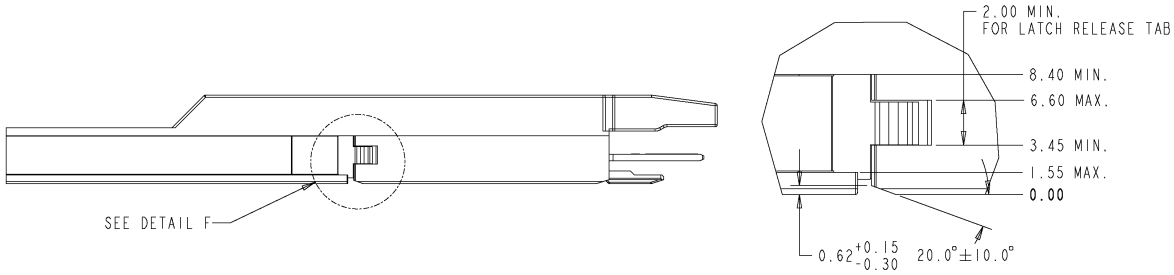


Figure 3-40: Latch pocket location

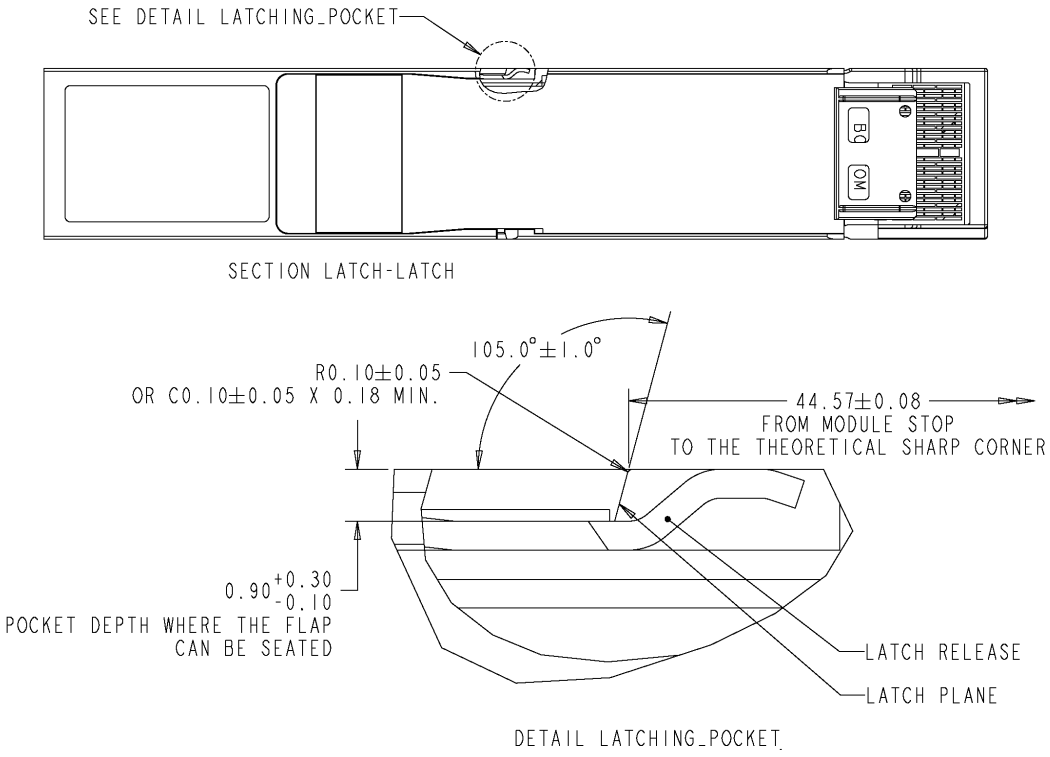


Figure 3-41: Latch release max width and latching pocket round

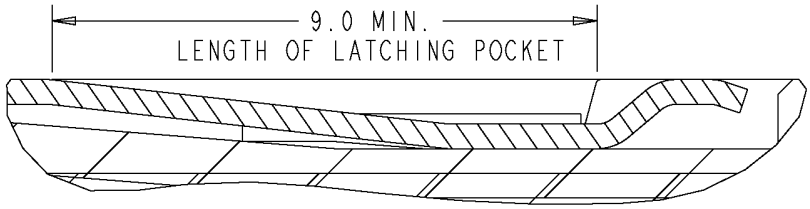


Figure 3-42: Latching pocket length

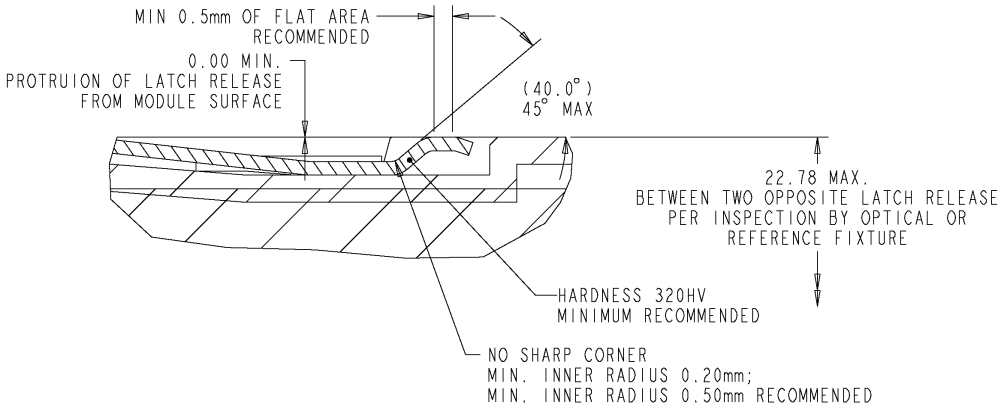


Figure 3-43: Latch plane corner radius and release details

Different latch release designs are allowed, as long as reliable latch release can be achieved.

3.11 Module Color Code

The module shall adhere to a color code by application of color to its pull-tab or other appropriate method. The color code to be applied is given in Table 3-3.

Table 3-3: OSFP-XD color code

Product Type	Example PMD	Color	Pantone Code (Recommended)
OSFP-XD copper cables	N/A	Black	N/A
OSFP-XD AOC cables	N/A	Grey	422U
OSFP-XD 850nm solutions	1600G-SR16	Beige	475U
OSFP-XD 1310nm solutions for up to 500m	1600G-DR16, DR8	Yellow	107U
OSFP-XD 1310nm solutions for up to 2km	1600G-4FR4, 2FR4	Green	354C
OSFP-XD 1310nm solutions for up to 10km	1600G-LR16	Blue	300U
OSFP-XD 1310nm solutions for up to 40km	1600G-ER16	Red	1797U
OSFP-XD 1550nm solutions for up to 80km	1600G-ZR16	White	N/A

3.12 Touch Temperature

Module surfaces outside of the cage must comply with applicable touch temperature requirements. If the temperature of the module case will exceed applicable short-term touch limits, then a means to prevent contact with the case during the handling of the module shall be provided. Refer to UL 62368-1 and NEBS GR-63.

4 Single Row Surface Mount Technology OSFP-XD Connector and Its Cage

In this section, the configuration of a single row SMT (Surface Mount Technology) connector and its cage are presented.

4.1 Overview

Figure 4-1 gives an overview of a 1x1, without a module but with a blank plug. Blank plug is an optional cover for the empty port. Figure 4-2 depicts a 1x1 cage with an OSFP-XD module in the fully inserted position.

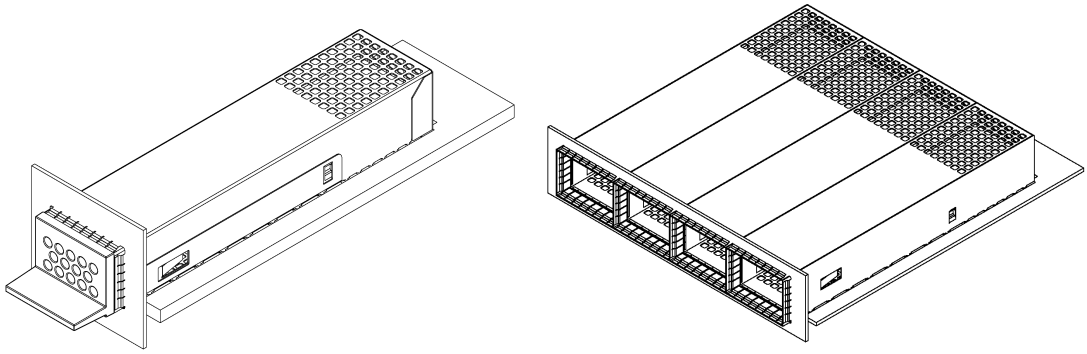


Figure 4-1: 1x1 cage, host PCB, panel, and blank plug

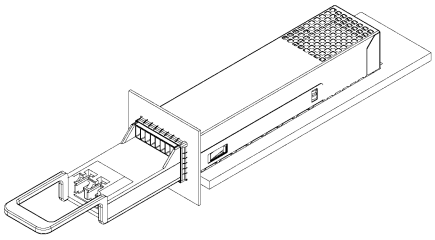


Figure 4-2: OSFP-XD module in a 1x1 cage

In the cage and connector mechanical drawings included throughout this specification, the datum as defined in Table 4-1 shall apply. For datum of the module, see Table 3-1.

Table 4-1: Descriptions of the cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 4-3
H	Seating plane of Cage on host pc board	Figure 4-3
J	Width of inside of Cage	Figure 4-4
K	Connector guide post #1	Figure 4-6; Figure 4-28
L	Cage Pin #1	Figure 4-3
M	Surface of the plated pads of the host board	Figure 4-16
N	Host pc board through hole #1 to accept Connector guide post	Figure 4-16
P	Host pc board through hole #2 to accept Connector guide post	Figure 4-17
R	Host pc board through hole #1 to accept Cage Pin	Figure 4-17
S	Width of Connector	Figure 4-28
T	Front surface of Connector	Figure 4-28
U	Seating plane of Connector, defined by the 4 connector standoffs	Figure 4-28

4.2 Cage Dimensions and Positioning Pin

Figure 4-3 through Figure 4-5 shows cage datum, positioning pin, port size and cage height. In addition, Figure 4-6 shows nominal dimensions between the module and the cage when the module is fully inserted. Note that the compliant pins in the cage are placed to support belly-to-belly applications.

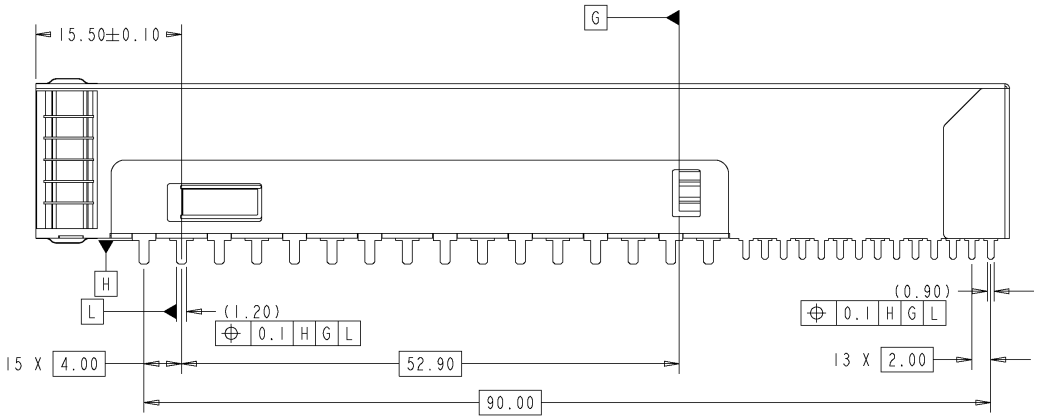


Figure 4-3: Cage positioning pins and forward stop

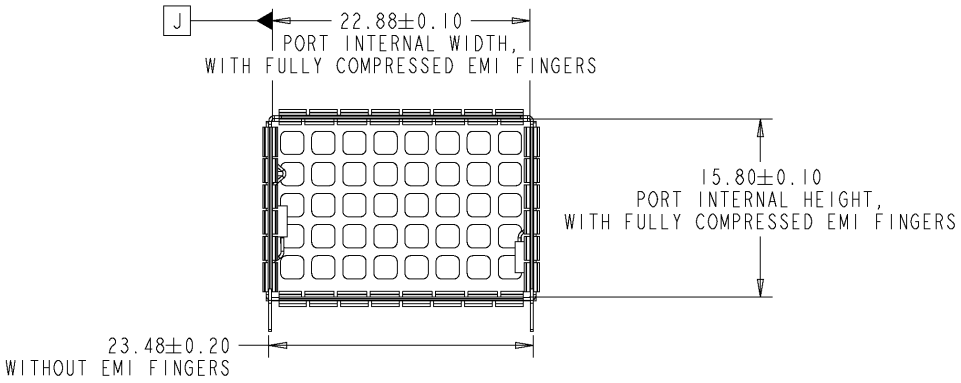


Figure 4-4: Port internal width and height

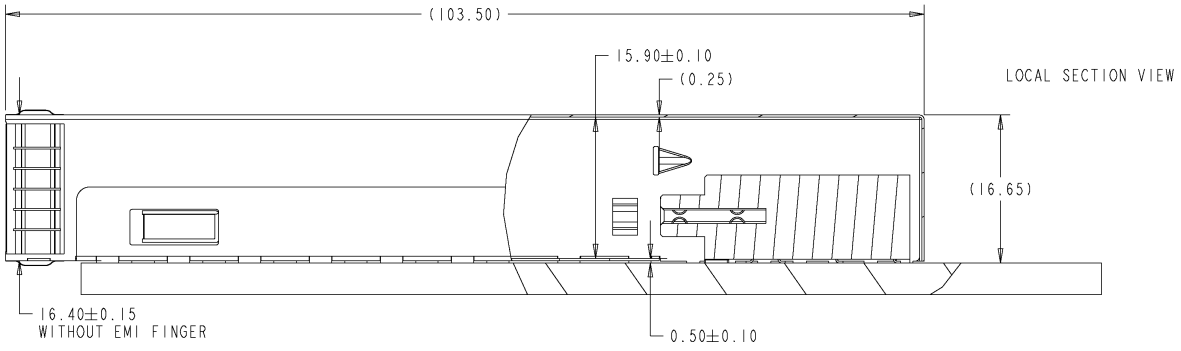


Figure 4-5: Side view of a 1x1 cage with vertical cage dimensions

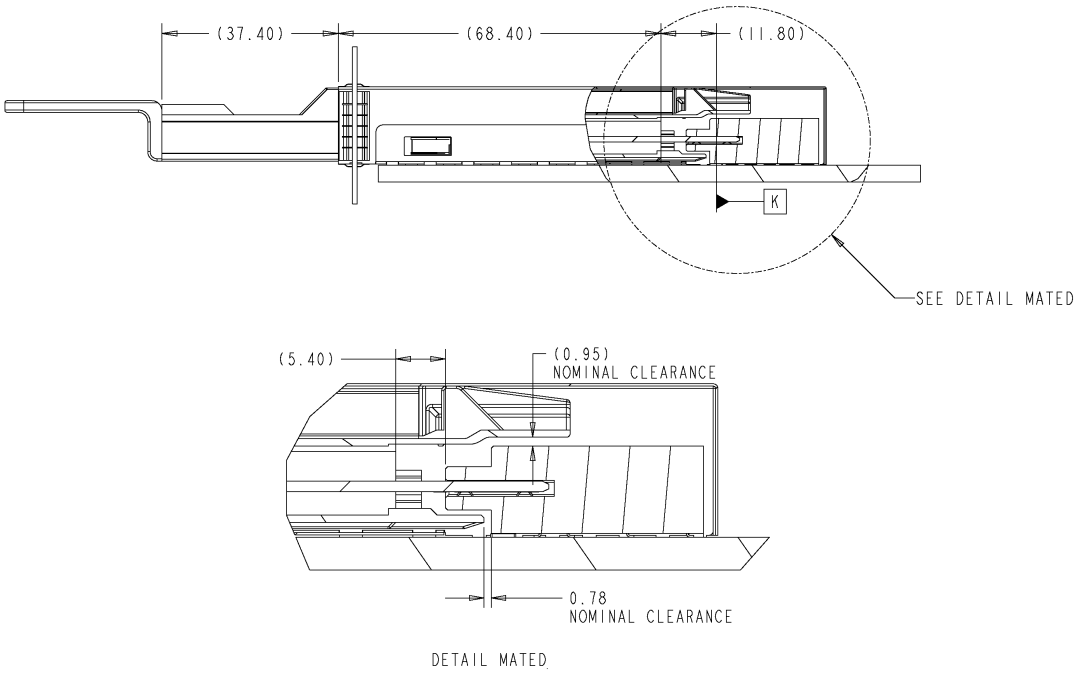


Figure 4-6: Side view of a 1x1 cage with axial reference dimensions

4.3 EMI Finger Pitches

Figure 4-7 gives EMI finger dimensions to be used for the internal side of top and bottom EMI fingers. Fingers for the left, right, and outside of the cage shall be designed to ensure appropriate EMI shielding, but finger pitch is not specified.

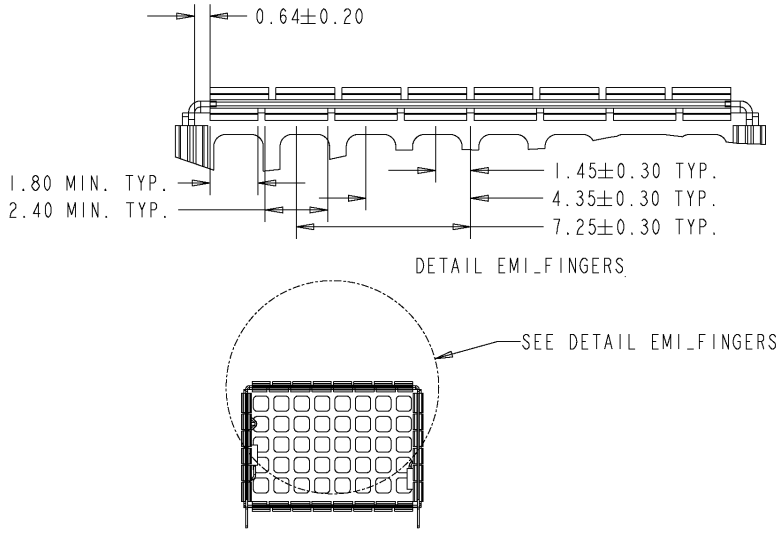


Figure 4-7: Internal EMI finger, top and bottom

4.4 Ventilation Hole

Cage should have ventilation holes as in the below figures to allow the airflow through the heatsink on the module. Rear ventilation holes are most crucial in terms of the airflow, while

the ventilation holes on the top also helps the airflow. Ventilation holes on the bottom of the cage also helps airflow, especially when used with the host PCB with cutout and module with airflow channel at the bottom.

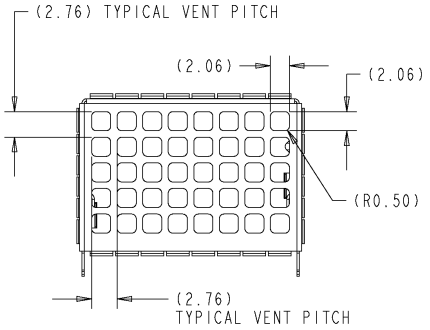


Figure 4-8: Rear ventilation holes

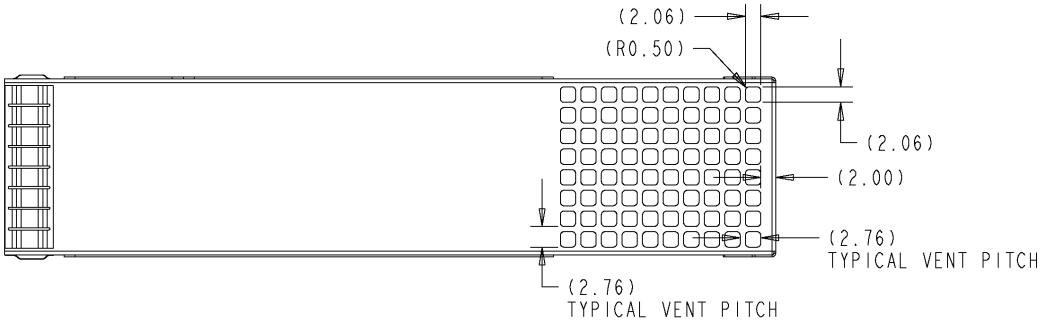


Figure 4-9: Top ventilation holes

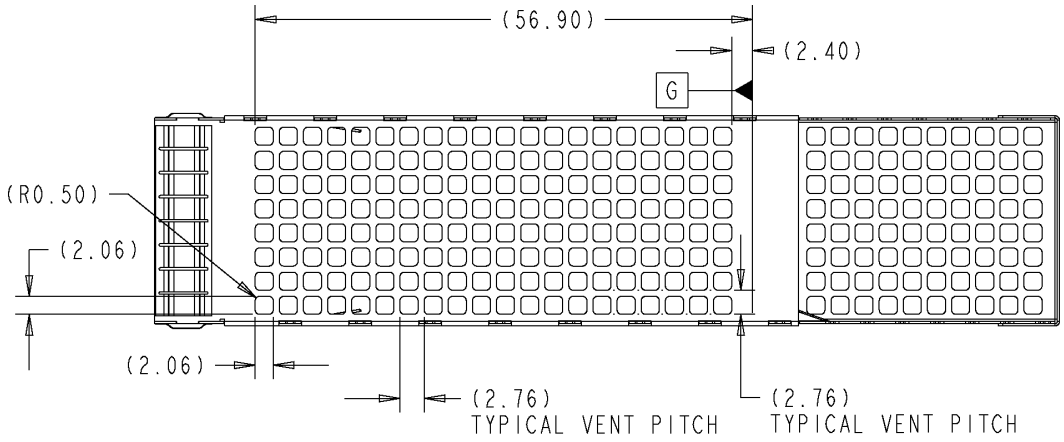


Figure 4-10: Bottom ventilation holes

4.5 Key and Stop

Figure 4-11 shows the key and forward stop features. Stop features engage with the forward stop of the module; they can be symmetric as shown, or placed asymmetrically within the given dimensions.

Figure 4-12 shows the keying feature, to prevent the insertion of the legacy OSFP modules.

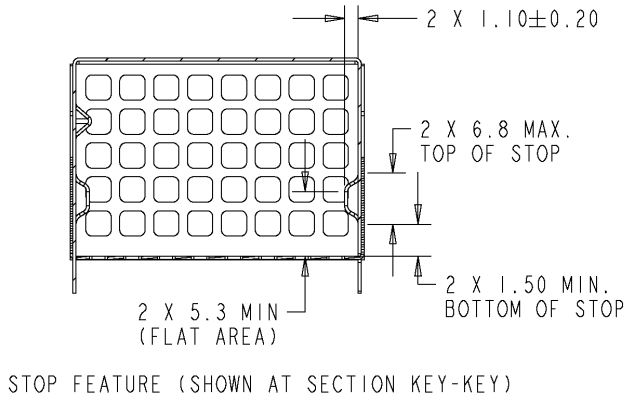


Figure 4-11: Cage stop feature

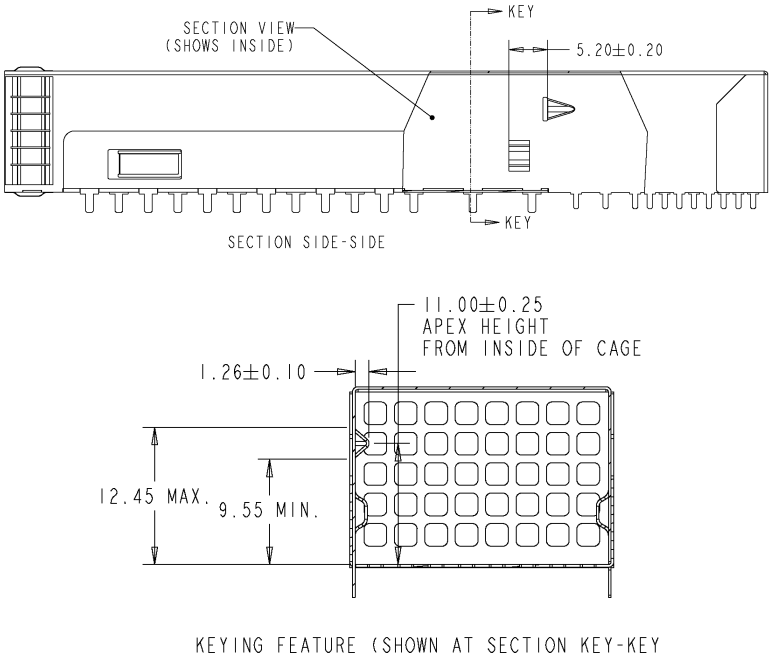


Figure 4-12: Cage keying feature

4.6 Extra Riding Heatsink

An OSFP-XD cage may have an extra riding heatsink as in the Figure 4-13. Figure 4-14 shows the cutout size of the cage for the extra riding heatsink. Figure 4-15 shows the reference design of the leading edge of an extra riding heatsink. The force which will be applied from the riding heat sink to an OSFP-XD module shall not exceed 36N downward.

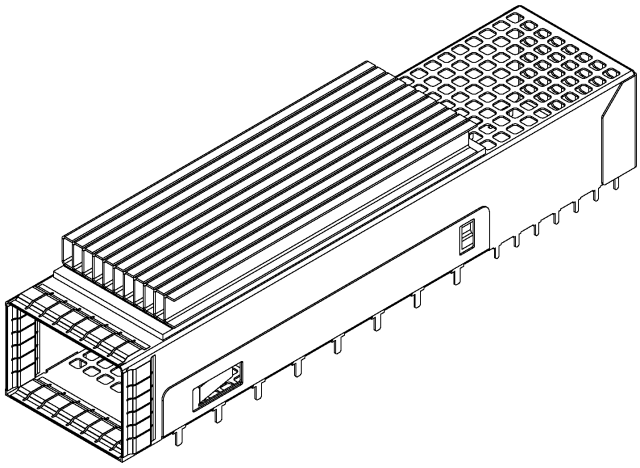


Figure 4-13: OSFP-XD 1x1 Cage with a riding heatsink

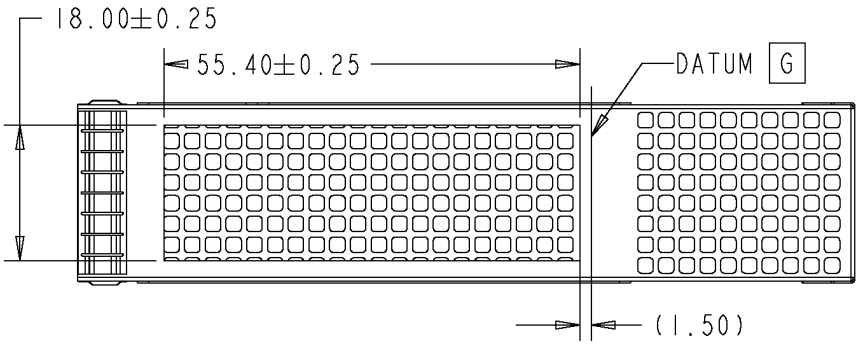


Figure 4-14: Cutout on the cage for a riding heatsink

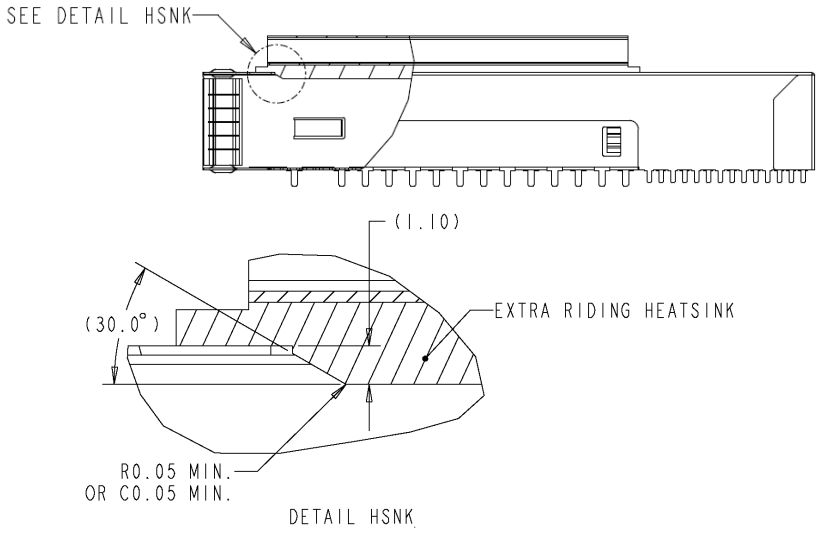


Figure 4-15: Heat sink leading edge, reference design

4.7 Host PCB Layout – 1x1 Cage

The host PCB layout pattern to accept a 1x1 cage is presented in this section.

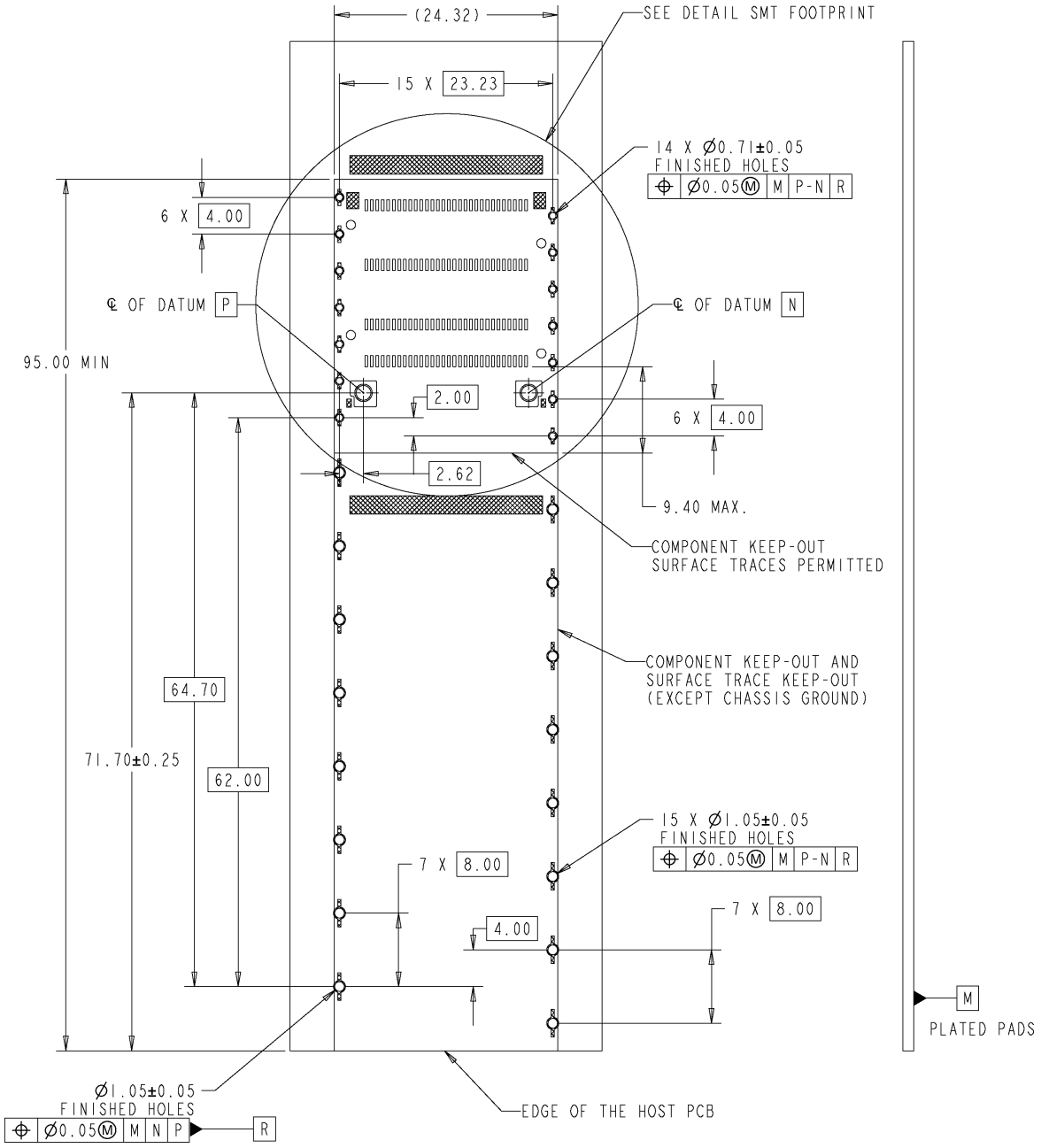


Figure 4-16: Host PCB layout for 1x1 cage

Figure 4-16 shows the footprint. Figure 4-17 shows the footprint near the SMT connectors. Compared to the OSFP or OSFP800 stacked SMT footprint, the cage and the connector are seated on the plated pads.

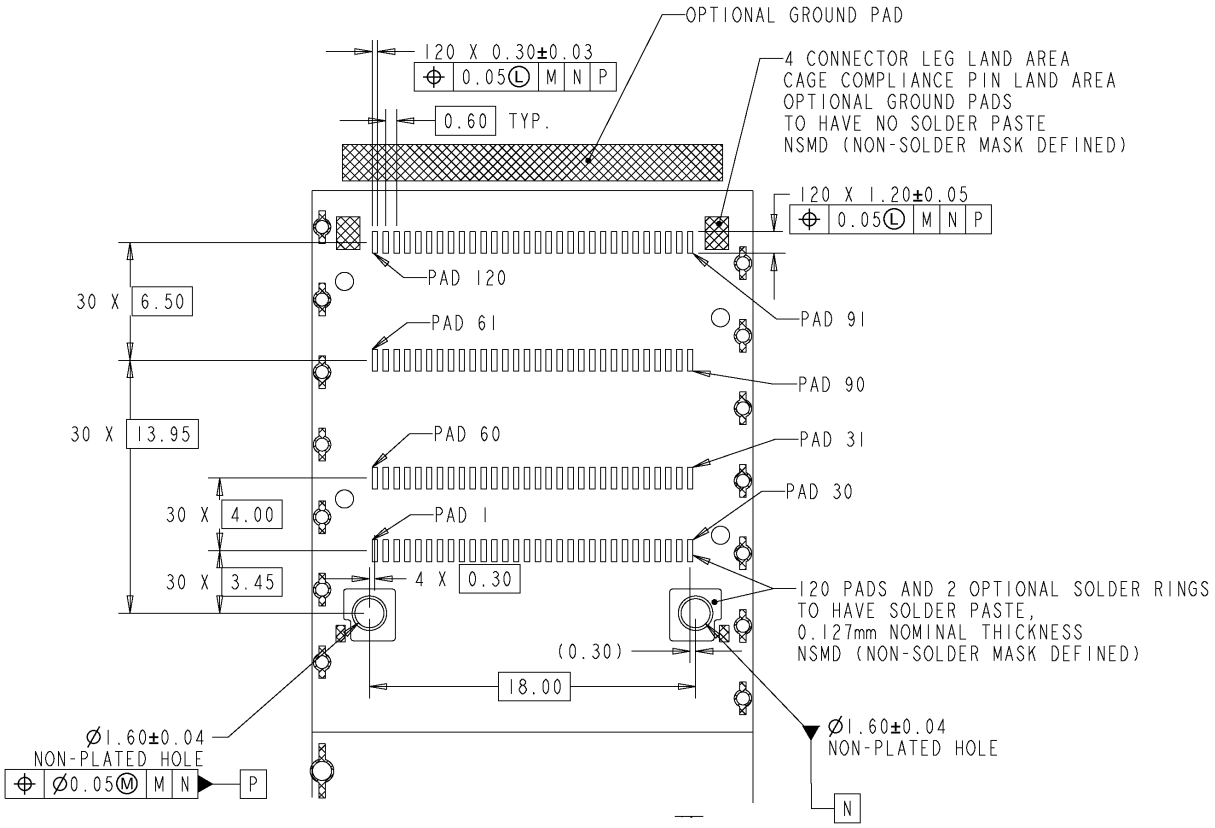


Figure 4-17: Host PCB layout (Detail SMT Footprint)

Figure 4-18 and Figure 4-19 show more details of the footprint. The solder rings are for SMT belly-to-belly applications. The cage and connector standoffs are placed on the plated pad without solder. In the Figure 4-19, where the plated pads for the connector standoff are too close to the cage compliance pin holes, the plated pad can be connected.

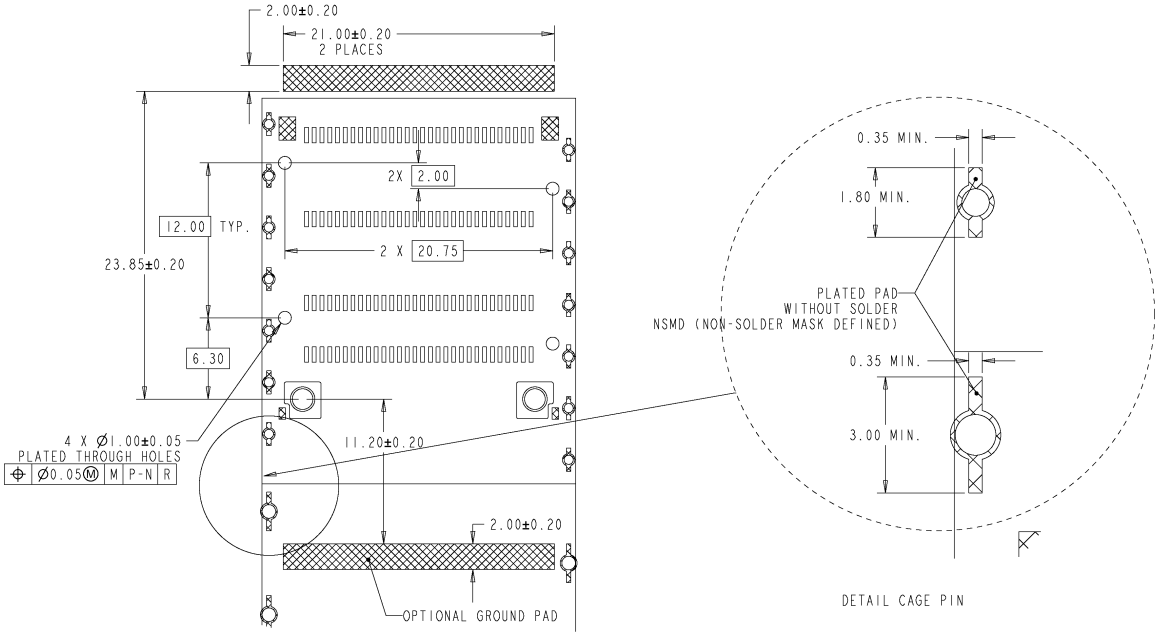


Figure 4-18: Optional ground pad and touchdown pad

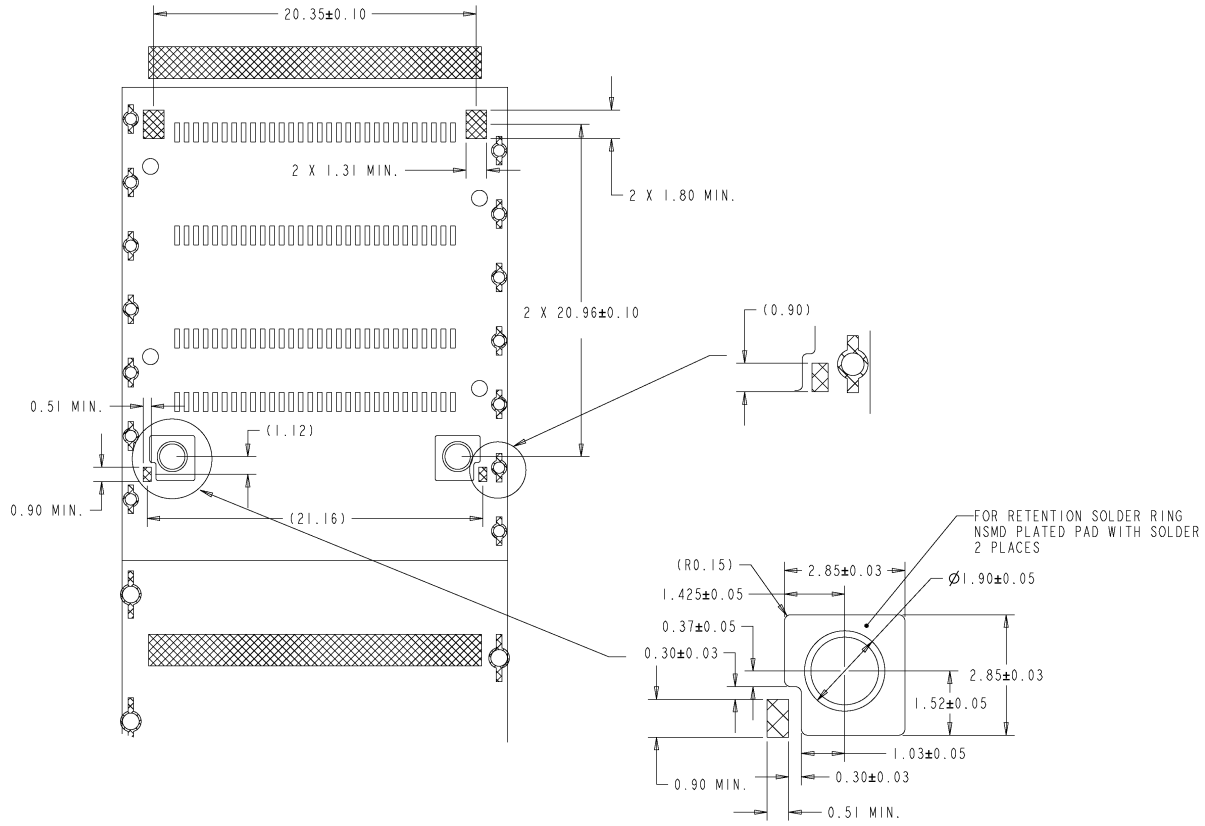


Figure 4-19: Solder ring and connector standoff touchdown pads

4.8 Host PCB Layout – Belly to belly application

Figure 4-8 shows host system footprint for the belly to belly application. There is minimum thickness on the host board. The cage and the connector which support the belly to belly application should be designed to support at least this minimum thickness of the board.

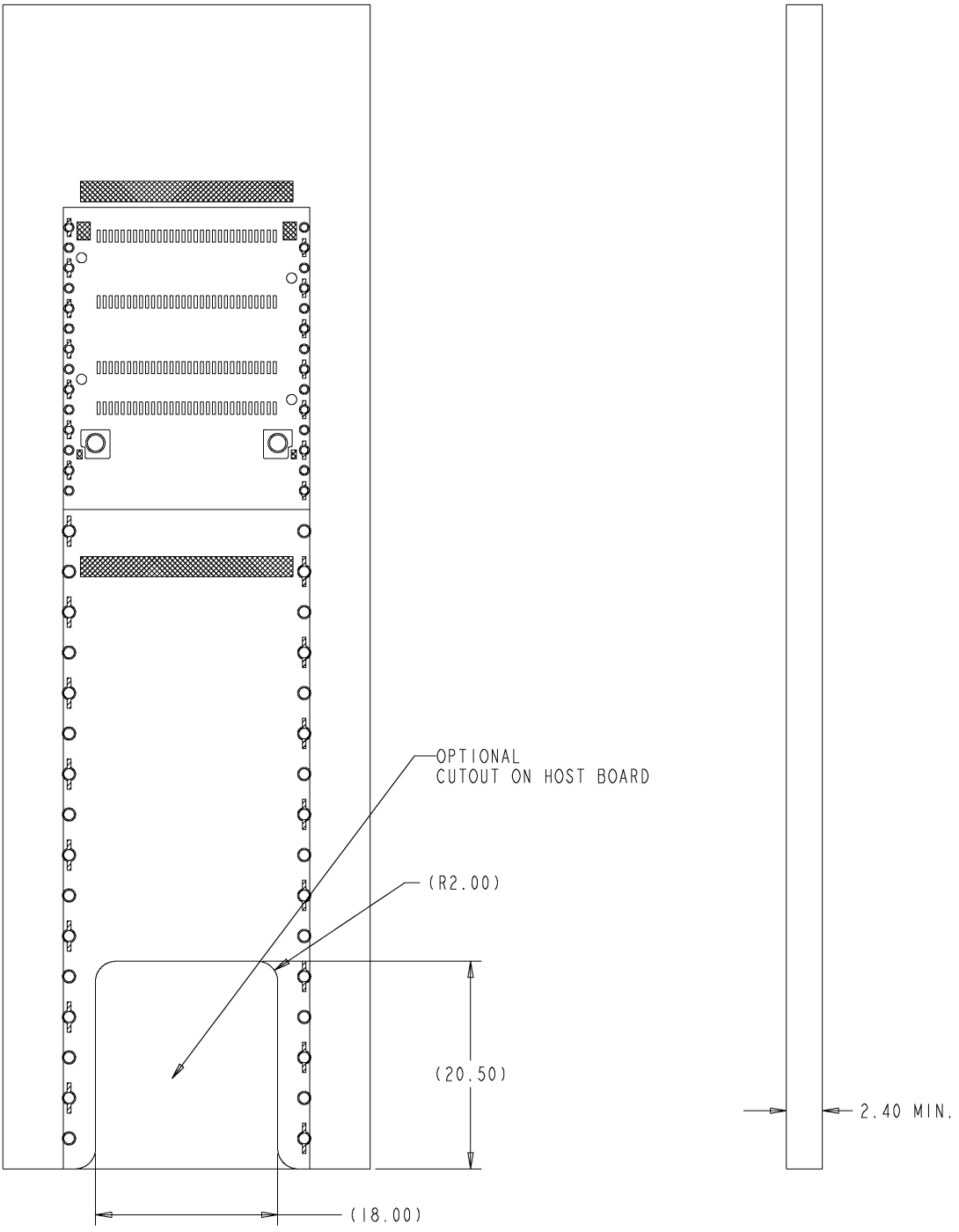


Figure 4-20: Belly to Belly 1x1 SMT PCB layout

Figure 4-20 also shows an optional cutout on the host board; this optional cutout can be applied to the belly to belly or single row case, to improve the airflow through the system.

4.9 Host PCB Layout – 1x4 Cage

For a 1x4 cage, the host PCB layout shall have a 23.23mm horizontal pitch. Figure 4-21 compares the host PCB layout between the 1x1, 1x2 and 1x4. The details of the 1x2 PCB layout are not given in this document.

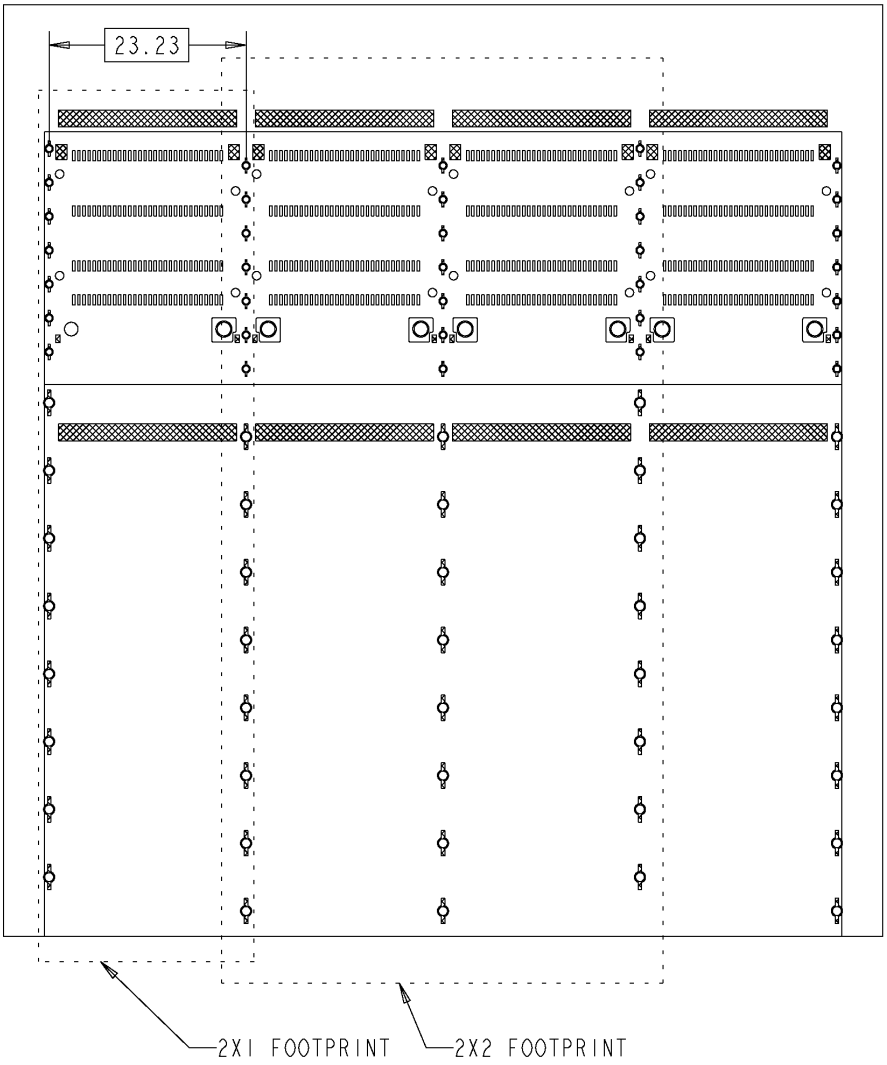


Figure 4-21: Comparison of host PCB layout between 1x1, 1x2 and 1x4

To ensure the belly to belly application without the compliance pin collision in the minimum thickness of the board, the length of the compliance pins should meet the specification as in the Figure 4-22.

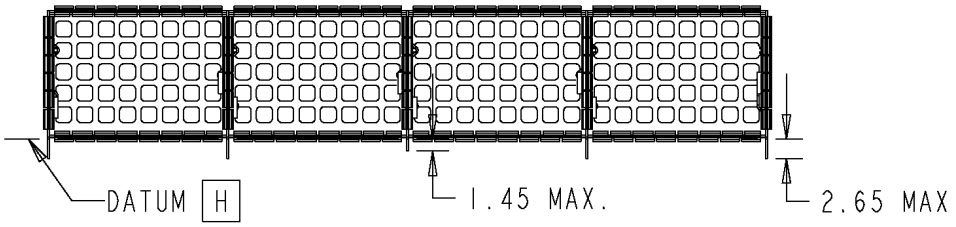


Figure 4-22: Compliance pin length, 1x4 Cage

4.10 Latch Flaps in Cage

In the cage, flaps as shown in Figure 4-23 and Figure 4-24 shall be on both sides of the cage to latch the module into the cage. Flaps are shown in a 1x1 cage but can be applied to a ganged cage such as a 1x4 cage or any 1xN cage.

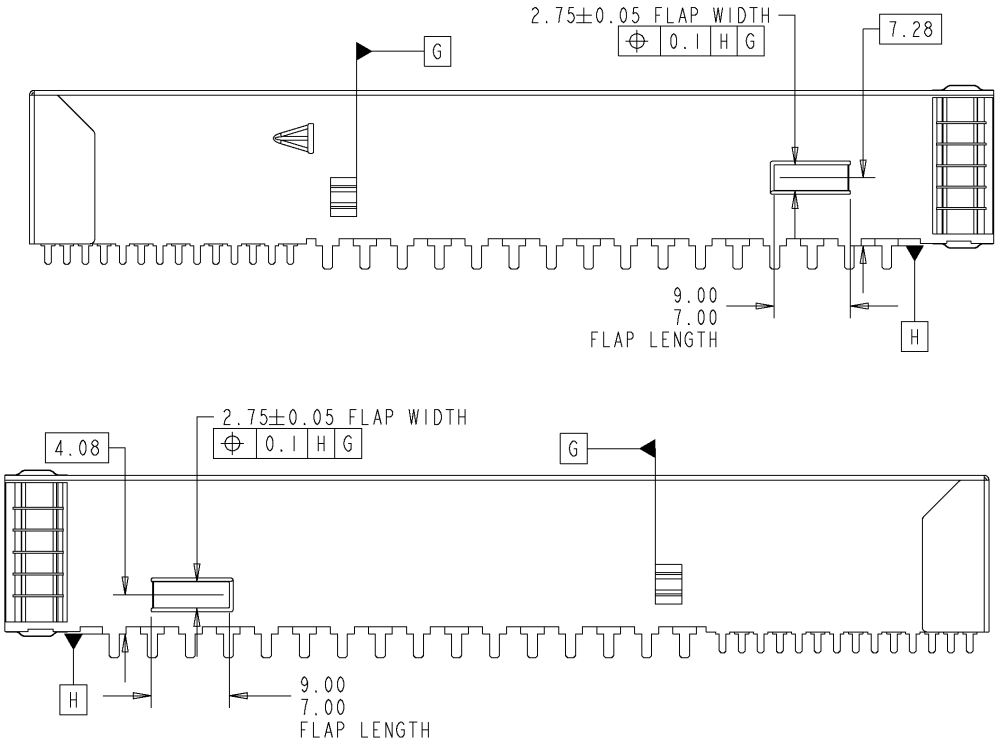


Figure 4-23: Latch feature, left and right side

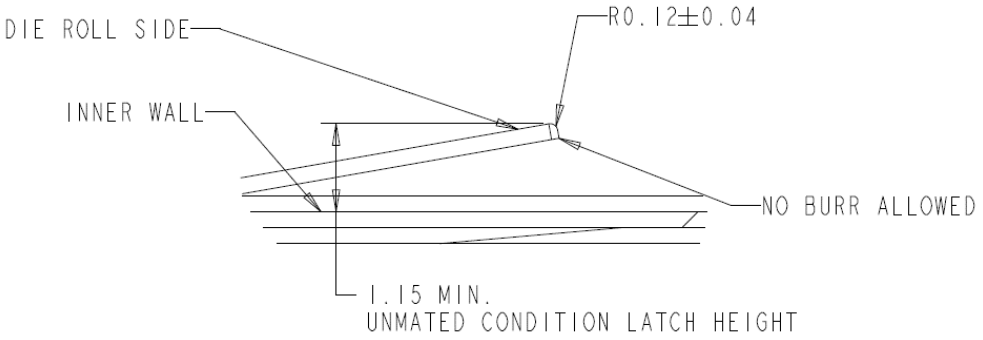


Figure 4-24: Latch flap, cross-sectional view from top

The cage latch flap shall be designed to meet the dimension 44.80mm, cage latch flap to module stop, when inspected to simulate the mated condition as in the Figure 4-25.

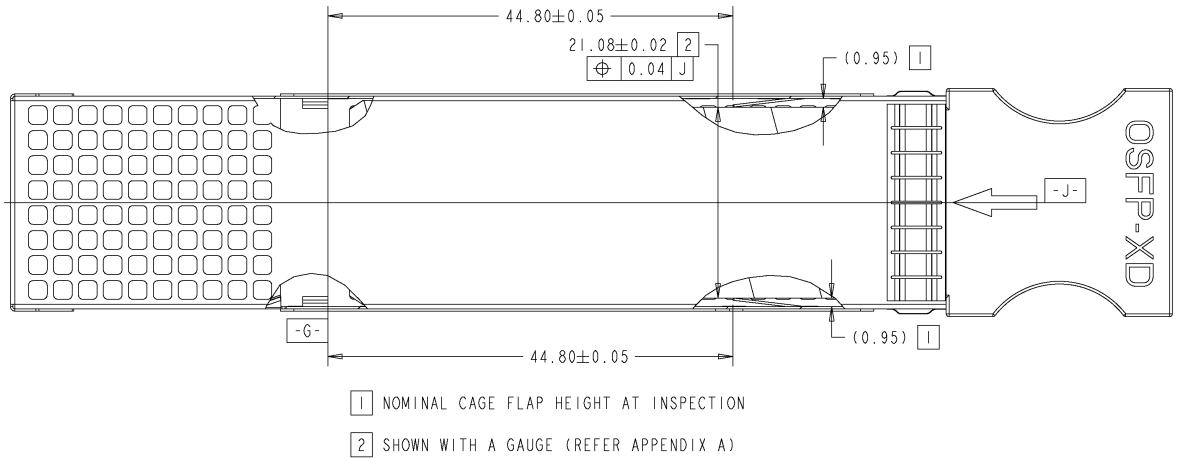


Figure 4-25: Latch flap, dimension from the positive stop

4.11 Bezel Panel Cut-Out

The EMI spring fingers of the cage shall make contact to the inside of the bezel panel cut out in order to make ground contact. Figure 4-26 and Figure 4-27 show recommended dimensions of the bezel panel cut-out. As the horizontal pitch of the cage is 23.23mm, the bezel cut out width of 1x shall be 47.51mm while the detailed design is not depicted here.

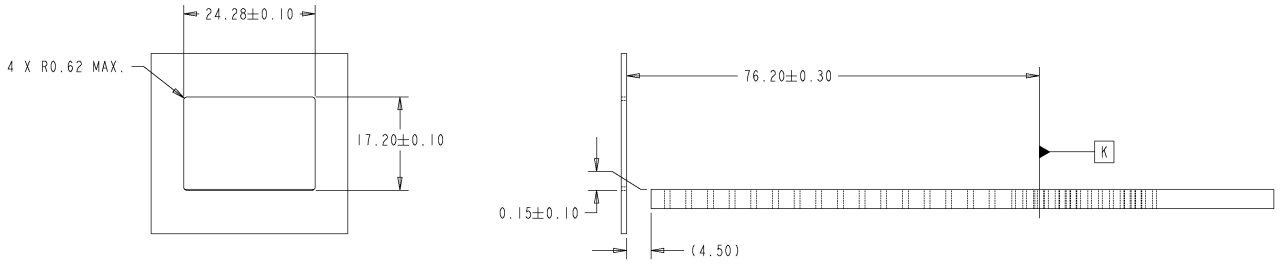


Figure 4-26: Bezel design and location for 1x1 cage

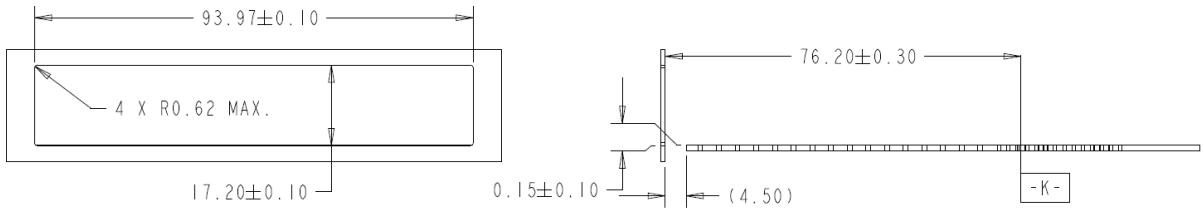


Figure 4-27: Bezel design for 1x4 cage

4.12 Single Row SMT Connector

The electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module to the outside. The tail direction of the connector is specified as shown.

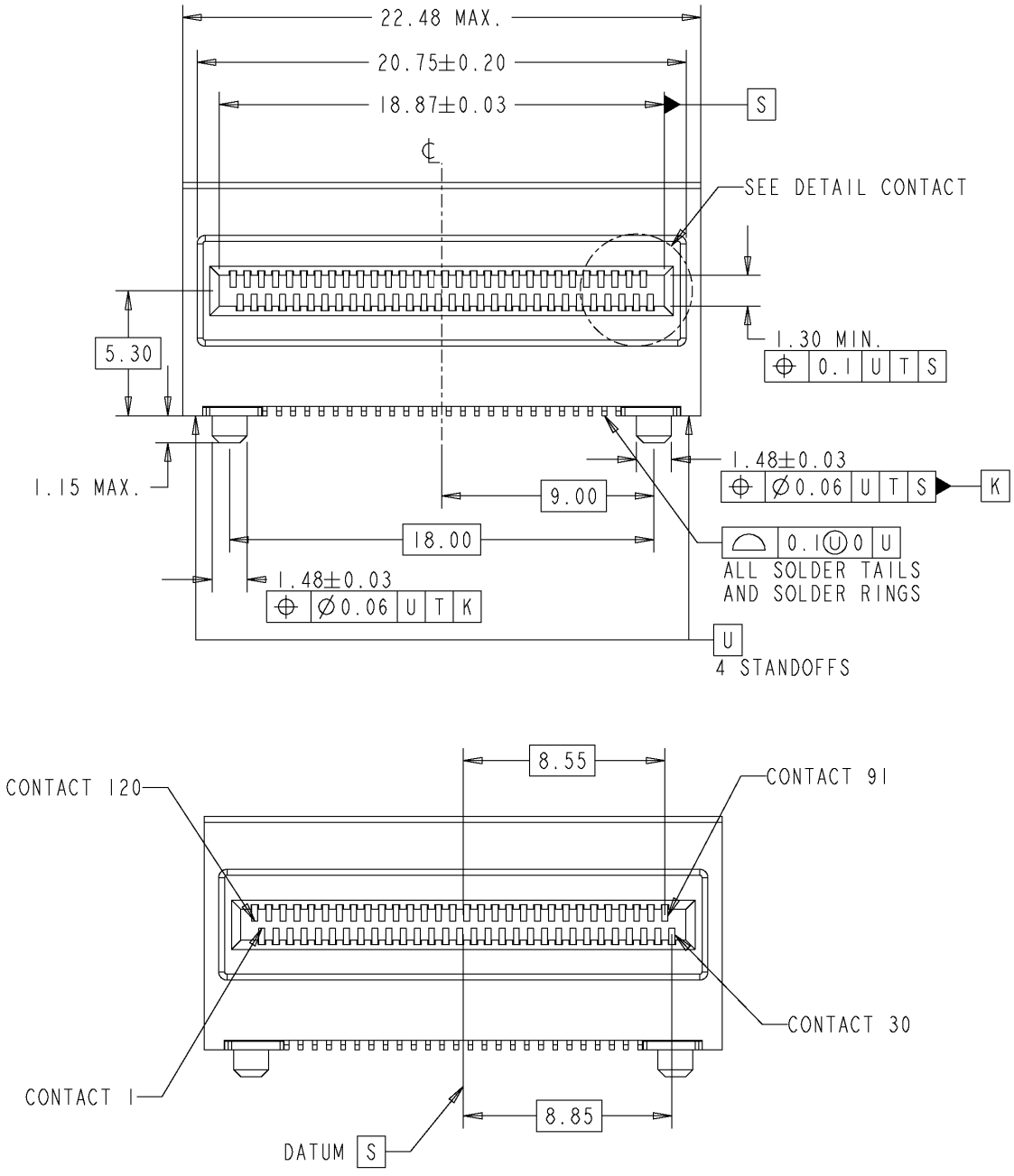


Figure 4-28: Surface mount connector

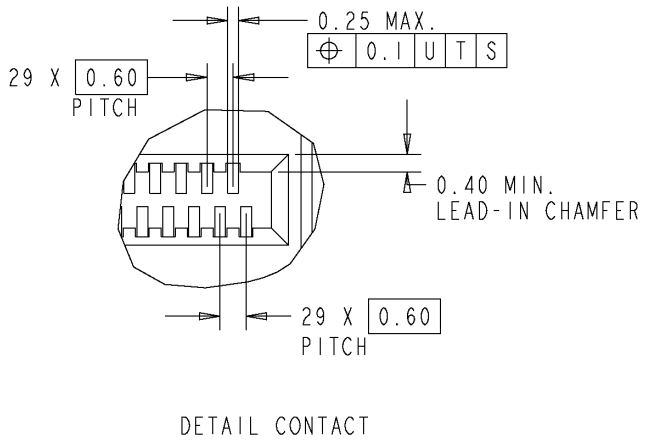
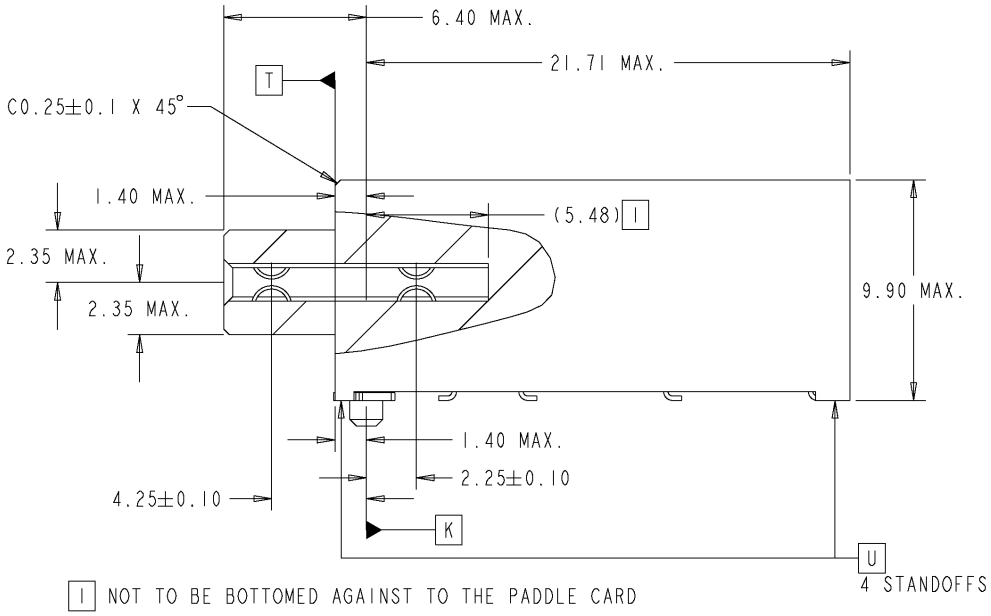


Figure 4-29: Surface mount connector, detail contact



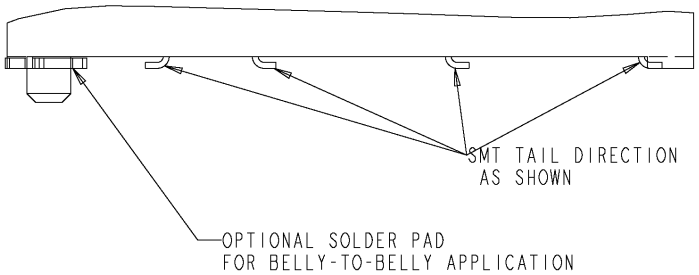


Figure 4-30: Surface mount connector, from the side view

4.13 Blank Plug

Any unused or empty port of a cage shall have a blank plug. The blank plug shall serve to minimize EMI while at the same time allowing for a maximum airflow no more than that of a module. See Figure 4-31 for a recommended design.

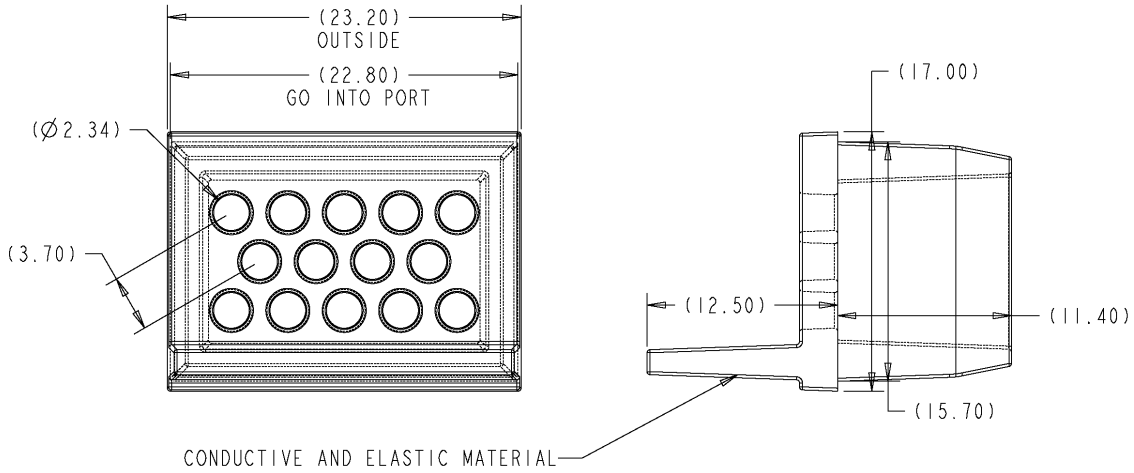


Figure 4-31: OSFP-XD blank plug (reference design)

5 Cabled Host Footprint for OSFP-XD

In this section, footprints for the cabled connectors are shown. Low speed signal and power are delivered through the host board and the compliance pin in the cabled connector, while the high speed signals will be transmitted through the cable.

The connector and the cage are not shown in this section but compatible with OSFP-XD modules. The mechanical feature of the connector and the cage will be compatible with the SMT connector and cage shown in the previous sections.

For single side application, two types of host PCB footprints, CHF-A (Cabled Host Footprint A) and CHF-B, are available. See Figure 5-1 to Figure 5-4 for the details of those footprints.

Figure 5-5 and Figure 5-6 show CHF-B2B (Cabled Host Footprint for Belly to Belly), which is for the belly to belly configuration for both sides with the cabled connectors. In CHF-B2B, one side is CHF-A and the other side is CHF-B to avoid interference.

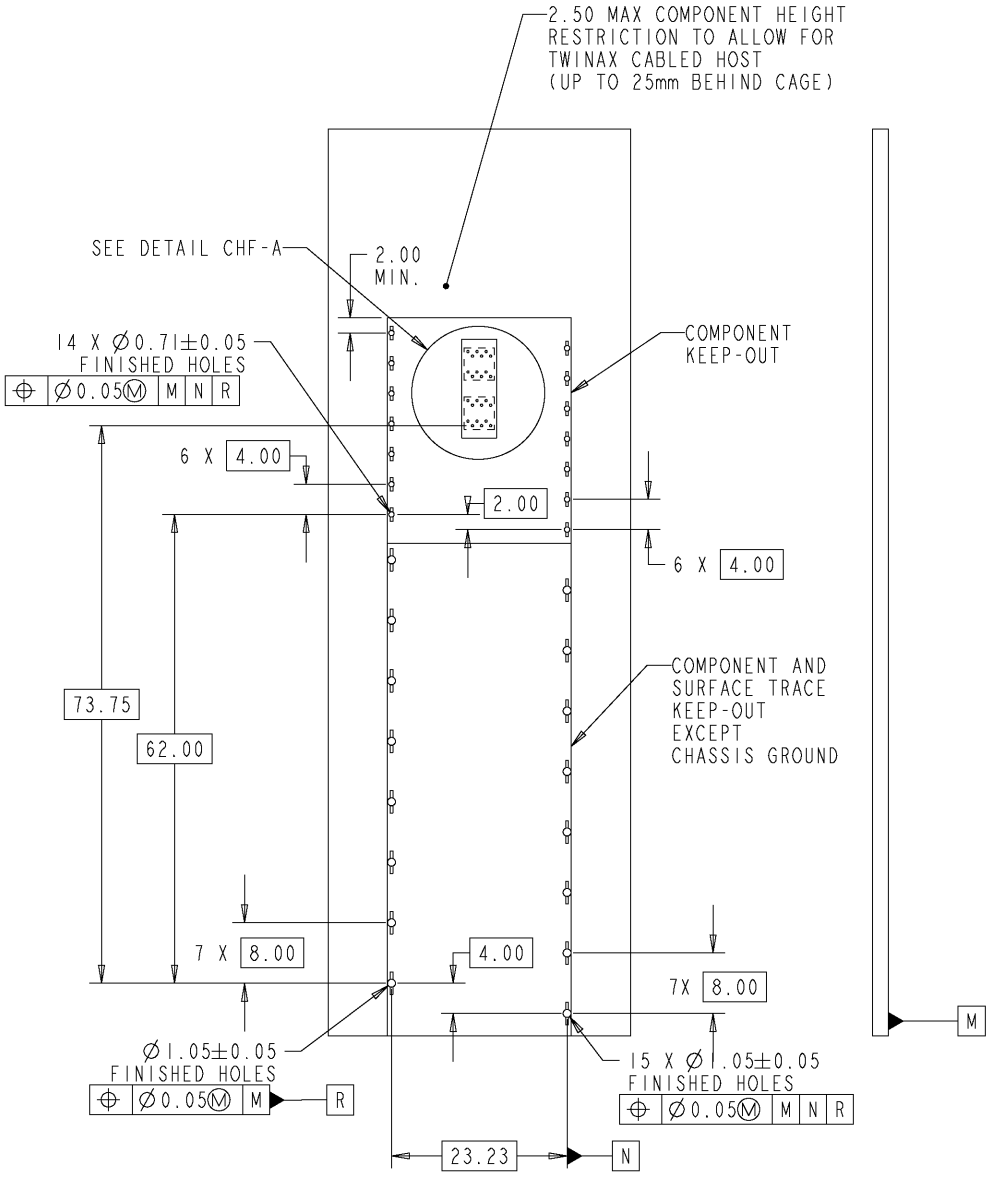


Figure 5-1: CHF-A (Cabled Host Footprint A)

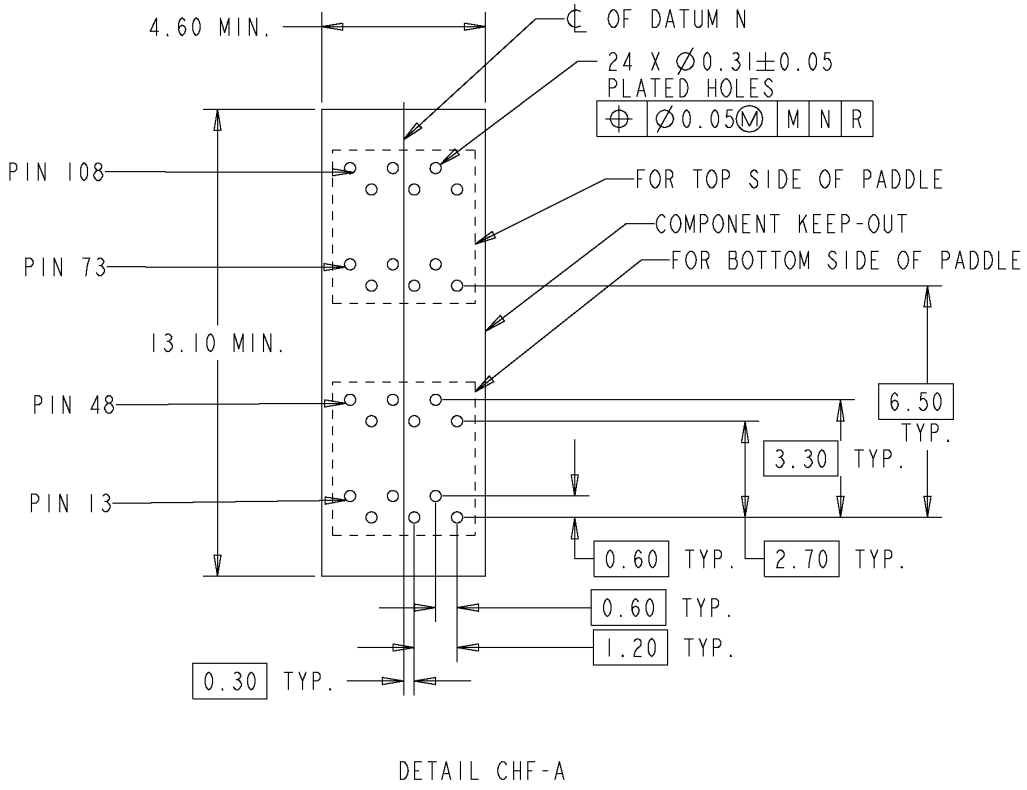


Figure 5-2: Detail of CHF-A

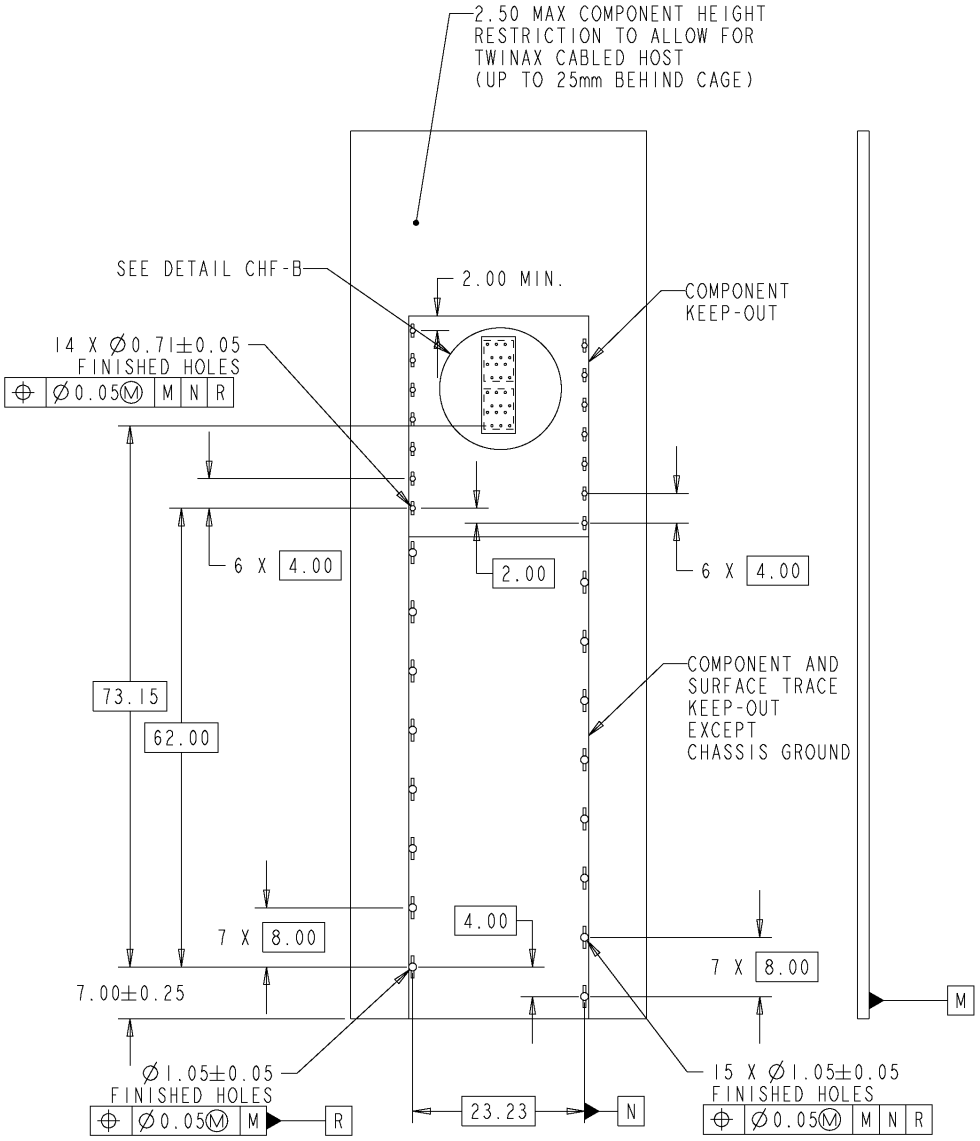


Figure 5-3: CHF-B (Cabled Host Footprint B)

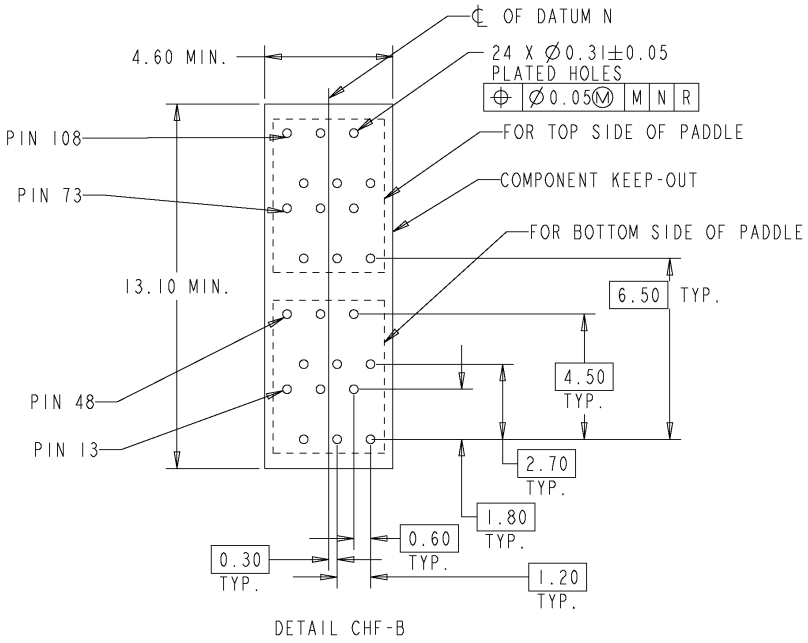


Figure 5-4: Detail CHF-B

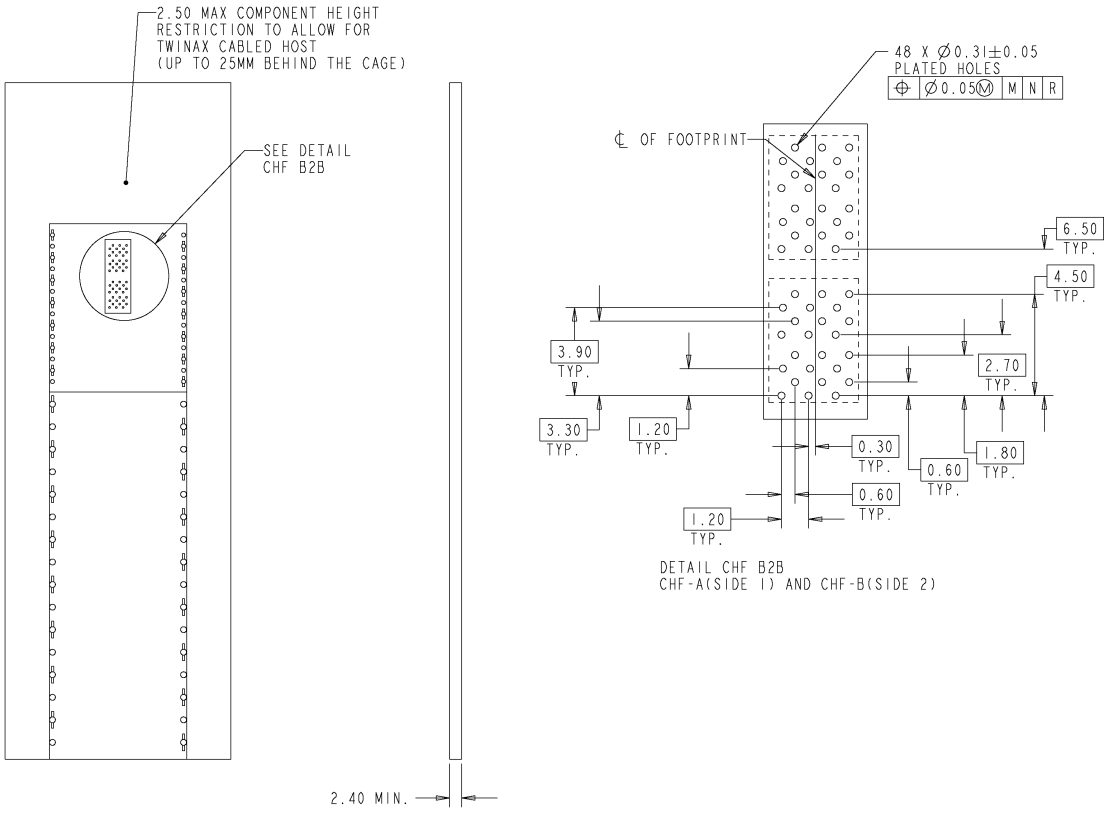


Figure 5-5: CHF-B2B (Cabled Host Footprint Belly to Belly)

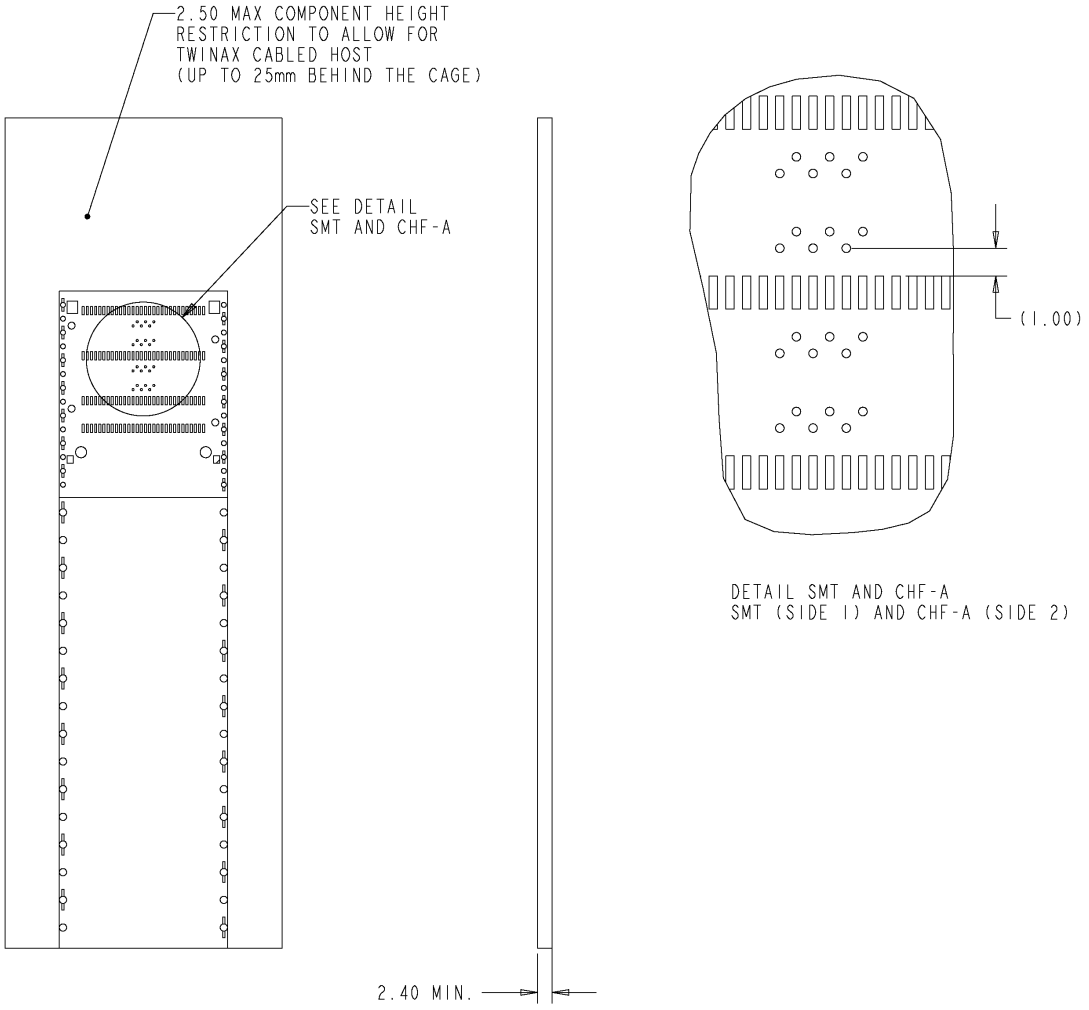


Figure 5-6: Belly to belly of SMT and CHF-A

6 Plug-in and Removal of an OSFP-XD Module

6.1 Insertion, Extraction, and Retention Forces for an OSFP-XD Module

Table 6-1: Insertion, extraction, and retention forces for an OSFP-XD module

Measurement	Minimum	Maximum	Units	Comments
OSFP-XD Module Insertion	N/A	50 (65)	N	Module to be inserted into connector and cage with latch mechanism engaged. (65N if the cage has riding heatsink)
OSFP-XD Module Extraction	N/A	40 (55)	N	Module to be removed from connector and cage with latching mechanism disengaged. (55N if the cage has riding heatsink)
OSFP-XD Module Retention in Cage	125	N/A	N	No functional damage to module, connector, or cage with latching mechanism activated. If the module has a pull tab, the pull tab and its attachment to the module is recommended to withstand up to 90N of the pulling under 55C.

6.2 Durability

The required number of insertion and removal cycles as applicable to the OSFP-XD module and its mating connector and cage are found in Table 6-2. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 6-2: Durability

Insertion/Removal Cycles into Connector/Cage	Minimum (cycles)	Comments
Module Cycles	50	Number of cycles for an individual module, to be tested with cage, connector, and module; latches may be locked out during testing
Connector/Cage Cycles	100	Number of cycles for the connector and cage with multiple modules, to be tested with cage, connector, and module; latches may be locked out during testing

7 Thermal Performance

7.1 OSFP-XD Module Thermal Requirements

The OSFP-XD module shall operate within one or more of the case temperature ranges defined in Table 7-1. The temperature ranges are applicable between 60m below sea level and 1800m above sea level.

The module supplier is responsible for defining a location in the module where the case temperature be measured or monitored. The location should be close to, and well-thermally-coupled to, the component with the least thermal margin. See Appendix C for further details.

Table 7-1: Temperature range classes

Class	Case Temperature
Standard	0 through 70°C
Reduced	20 through 60°C
Extended	-5 through 85°C
Industrial	-40 through 85°C
Custom	Custom temperature range. Module shall be able to post temperature range to host via management interface.

Table 7-1 defines case temperature only. For reference, touch temperature is controlled by regulatory requirements for handling and incidental contact defined section 3.12.

7.2 OSFP-XD Connector Thermal Requirements

The OSFP-XD connector is required to achieve the following thermal requirements while sustaining maximum power as defined in section 10.6.

*Table 7-2: OSFP-XD Connector Thermal Requirements**

Parameter	Value
Life Expectancy	10 years
Maximum Ambient Temperature	65 °C
Maximum Temperature Rise of connector when all signal and power contacts energized simultaneously	30 °C

*Per EIA-364-70

7.3 OSFP-XD Module Airflow Impedance Curve

Figure 7-1 shows a typical airflow impedance range of an OSFP-XD, when it is tested in the impedance test jig as described in the section 7.4. This typical range of airflow impedance can be used as a reference in an OSFP-XD module's heat sink design and system design.

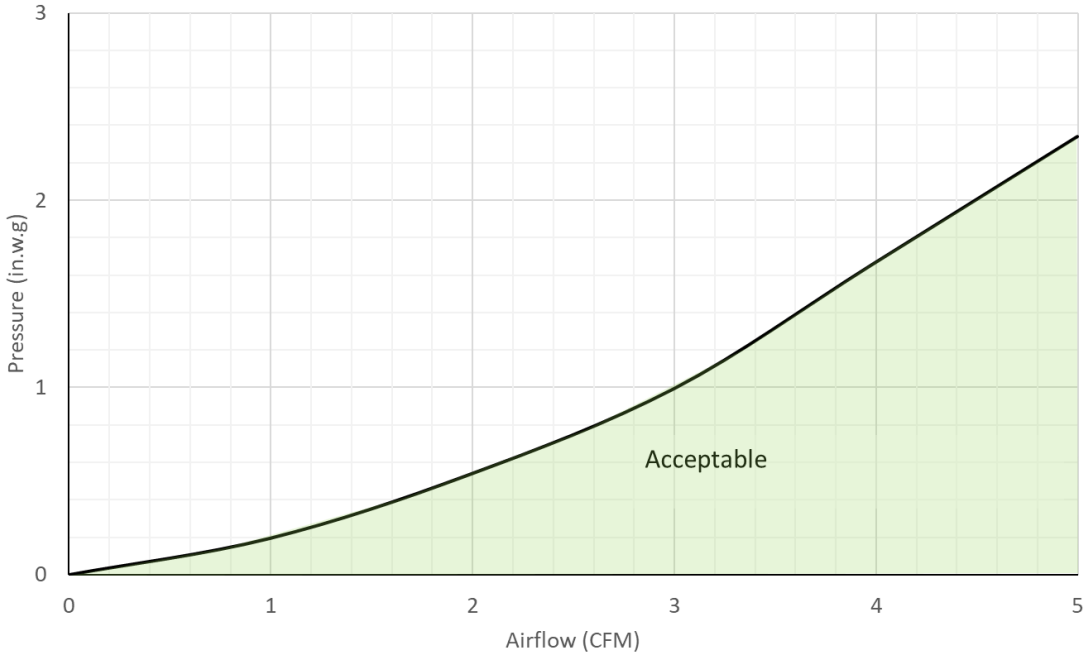


Figure 7-1: Target range of impediment to airflow of an OSFP-XD module

For the module which have maximum power of 20W or less, the impedance requirement can be relaxed as shown in the Figure 7-2. This will allow the module which have relatively low power can have more internal volume.

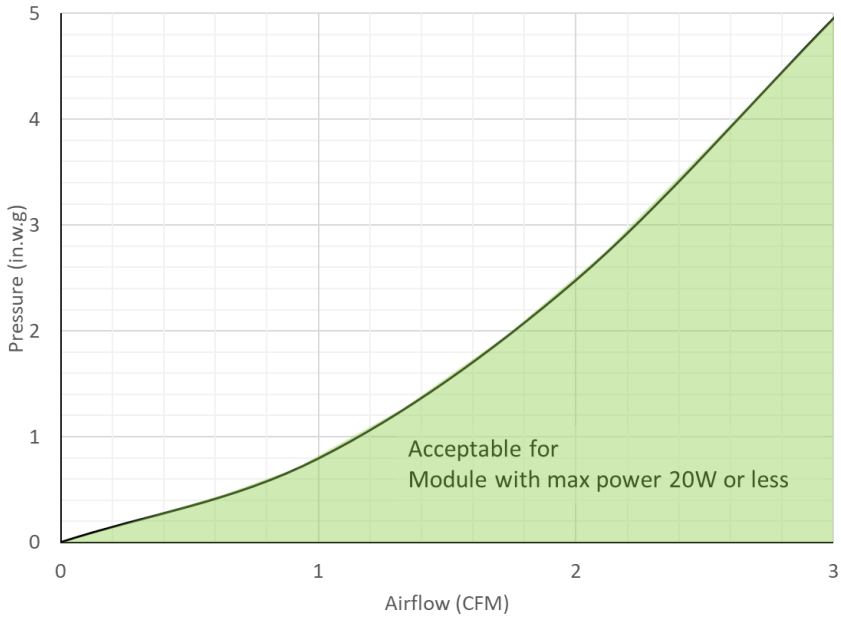


Figure 7-2: Target range of impediment to airflow of an 20W or less OSFP-XD module

7.4 Module Airflow Impedance Test Jig

The impedance range of Figure 7-1 was created using a jig as shown in Figure 7-3 and Figure 7-4. The jig is designed to support airflow along the heat sink as well as leakage around the module. The positive stop located within the jig reproduces the assembled condition within a host port. For a Type 2 module, it is normal for the front of the module to protrude beyond the jig opening. A Type 3 module may or may not extend beyond the jig opening.

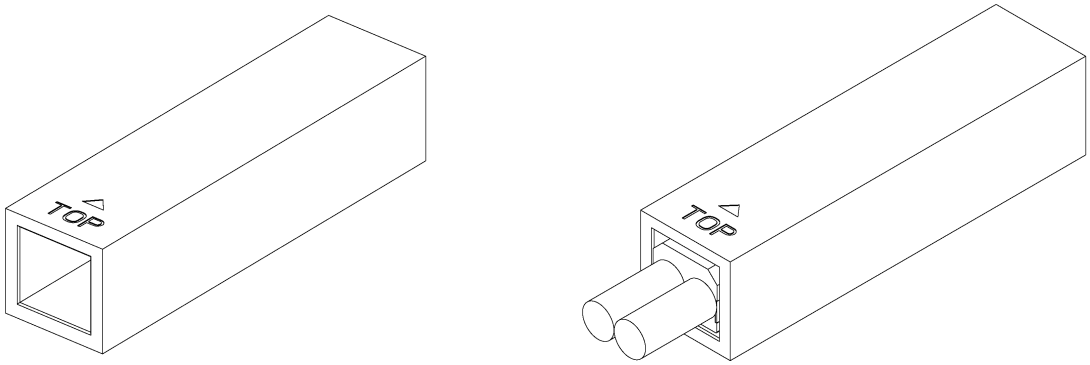


Figure 7-3: Impedance test fixture, with and without OSFP-XD module

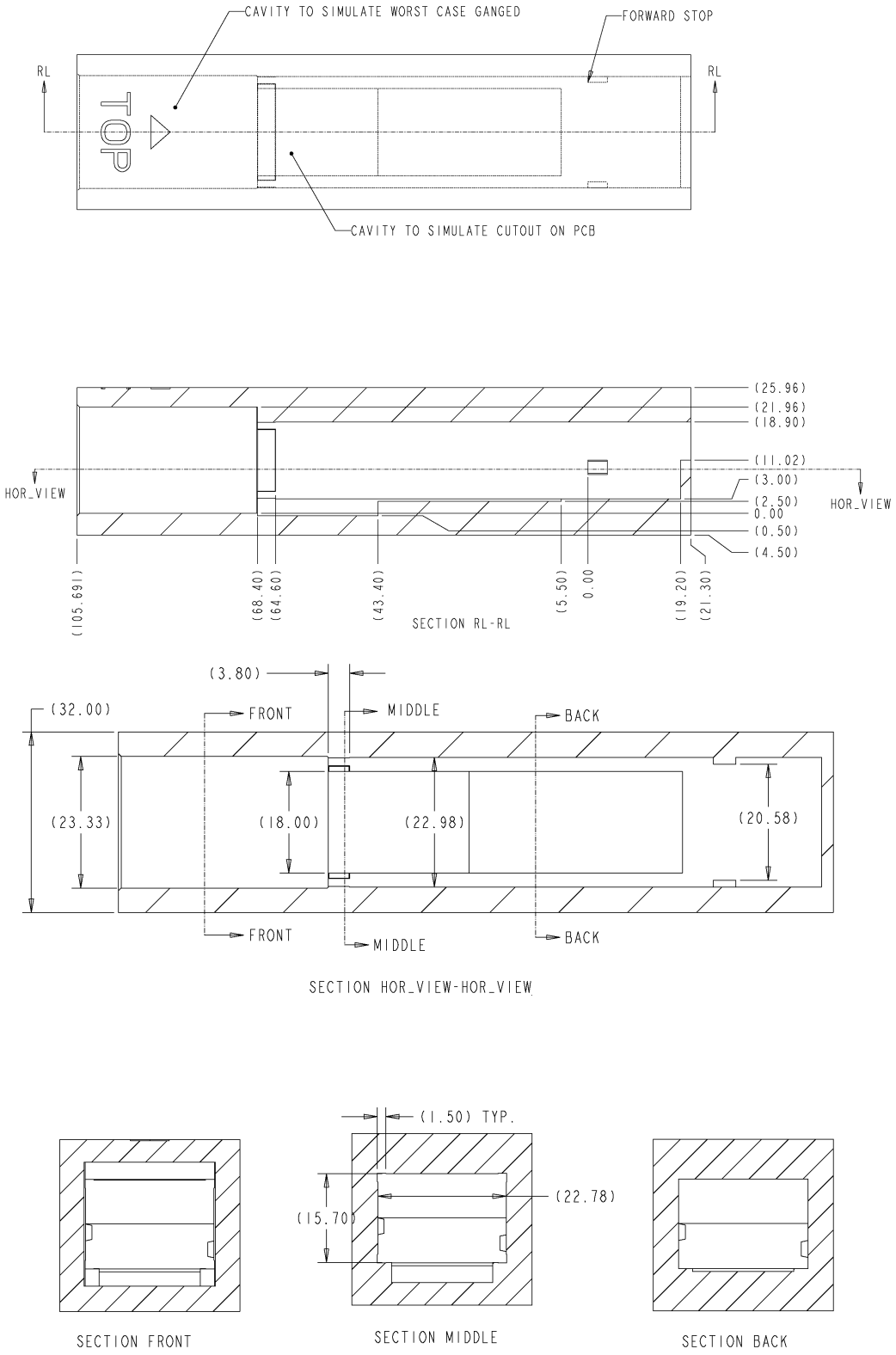


Figure 7-4: Detail dimensions of the impedance test fixture

8 OSFP-XD Riding Heat Sink Module and Cage Mechanical Specification

8.1 Overview

OSFP-XD Riding Heat Sink (OSFP-XD-RHS) is a 10.5mm high pluggable module which does not have an integrated heat sink as shown in the Figure 8-1 and Figure 8-2. In place of OSFP-XD's integrated heat sink, OSFP-XD-RHS cage shall have a riding heat sink. To prevent insertion of OSFP-XD-RHS into a standard OSFP-XD cage, the shape and location of the positive stop has been changed. See Table 8-1 for a comparison between the OSFP-XD-RHS and OSFP-XD.

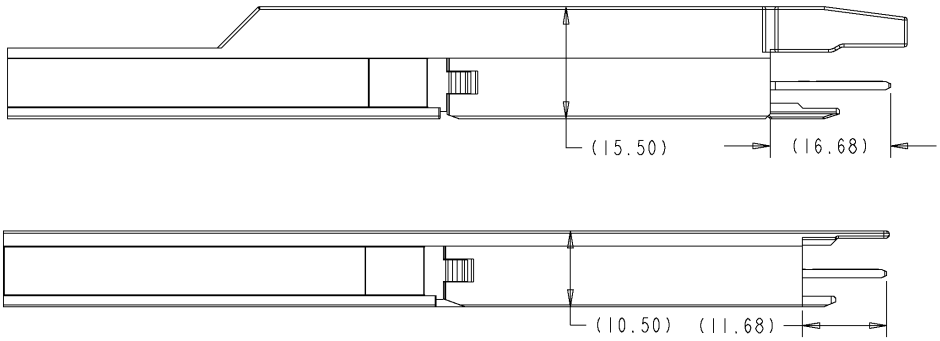


Figure 8-1: Side view of a typical OSFP-XD (top) and a typical OSFP-XD-RHS (bottom)

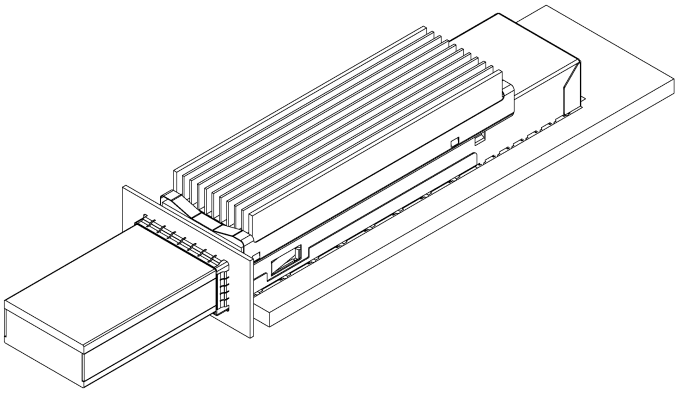


Figure 8-2: OSFP-XD-RHS in its cage

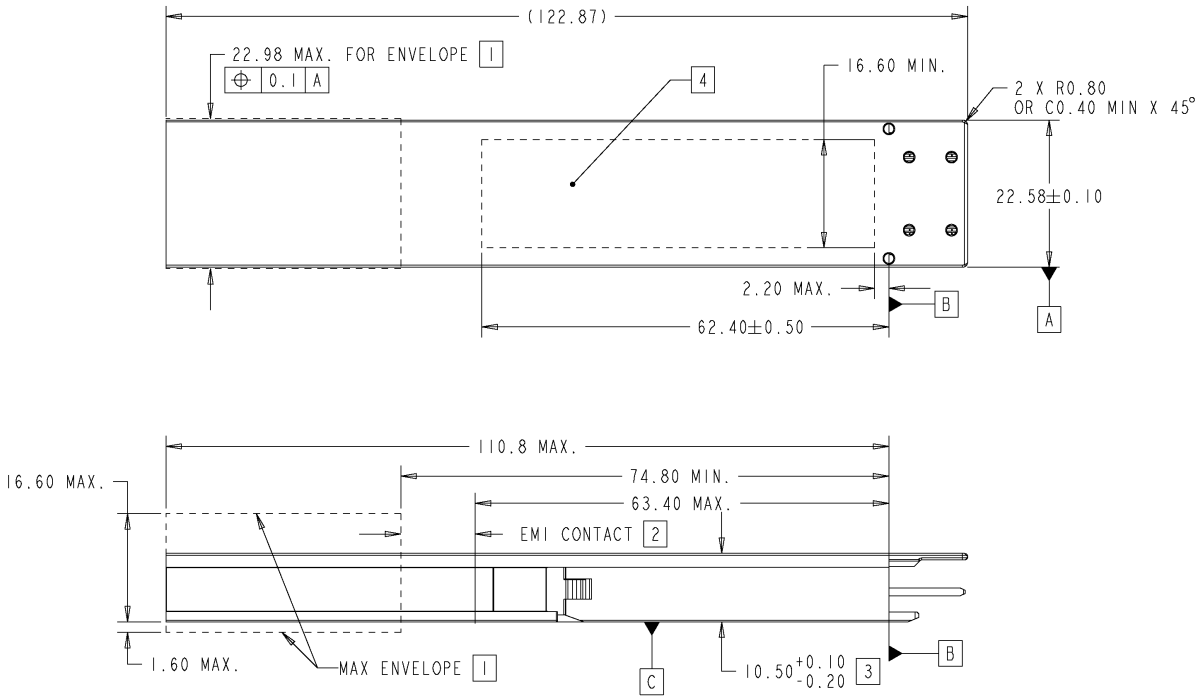
Table 8-1: Comparison of OSFP-XD-RHS to OSFP-XD

OSFP-XD-RHS feature	Comment
Module	10.5mm height without heat sink and different positive stop; for the feature which is not explicitly specified for OSFP-XD-RHS, same specification as of OSFP-XD shall be applied.
Connector	Identical with Surface Mount Connector
Host PCB Board Layout	Identical with Surface Mount type
Cage	Port height/positive stop/bezel cutout is different with OSFP-XD
Insertion/Extraction/Retention	No change; see Table 6-1
Durability	Requires testing with riding heatsink; see Table 8-3.
Thermal Requirement	Identical with OSFP-XD
Airflow Requirement	Not applicable (Section 7.2 is not applied)
Electrical and Management interface	Identical with OSFP-XD

In the following sections, the dimensions of the OSFP-XD-RHS will be defined.

8.2 OSFP-XD-RHS Module Mechanical Specification

Figure 8-3 shows the overall dimension of an OSFP-XD-RHS module from a top view. The reference datum definition is identical with Table 3-1, but note that the location of the datum B (forward stop of the module) is shifted 5mm to prevent an OSFP-XD-RHS from being fully inserted into an OSFP-XD cage as described in section 4 or 5.



1 FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN BE EXTENDED 1.60mm MAX FROM THE BOTTOM 16.60mm MAX FROM THE BOTTOM WITH UP TO 22.93mm WIDTH IN THE MAX ENVELOPE SHOWN.

2 INDICATED SURFACE (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

3 APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

4 SURFACE TO BE THERMALLY CONDUCTIVE.

Figure 8-3: Overview of the OSFP-XD-RHS and heat sink contact area

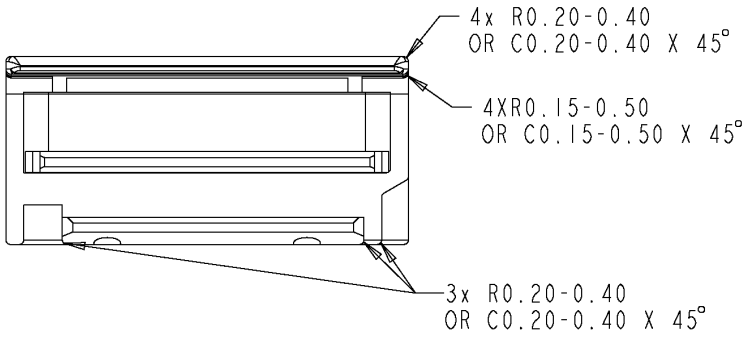


Figure 8-4: Corner radius of OSFP-XD-RHS in back view

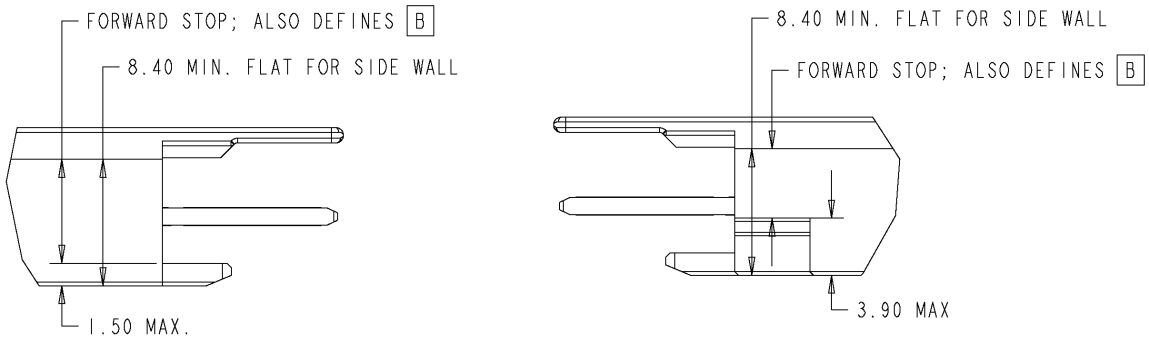


Figure 8-5: OSFP-XD-RHS forward stop

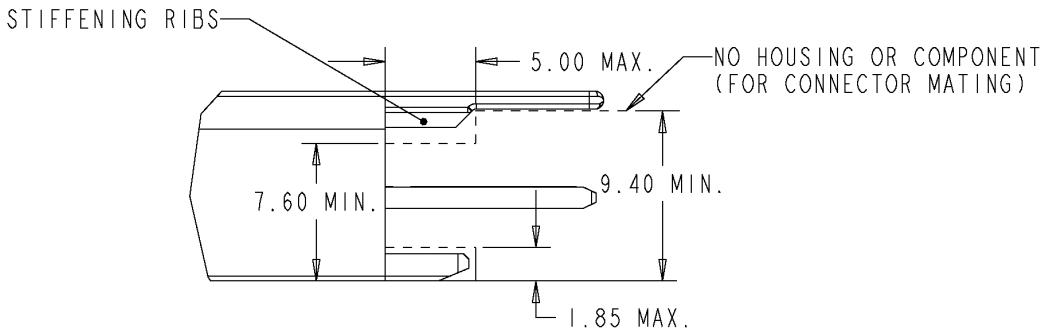


Figure 8-6: Connector keepout area from the side view

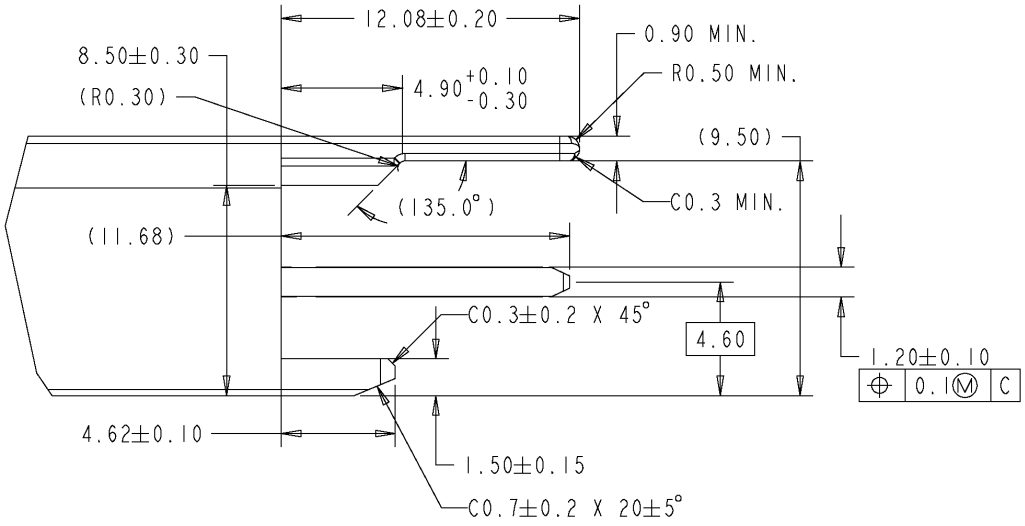


Figure 8-7: OSFP-XD-RHS, back of the module

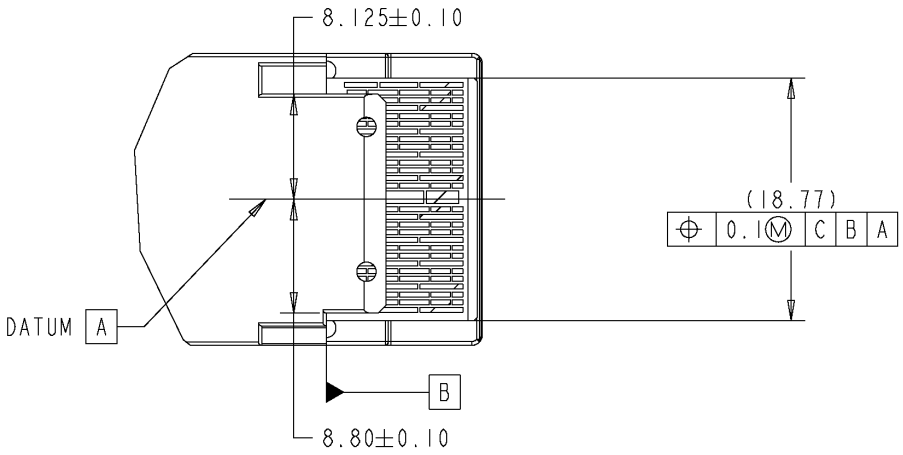


Figure 8-8: Paddle card position (bottom view of module) and module width

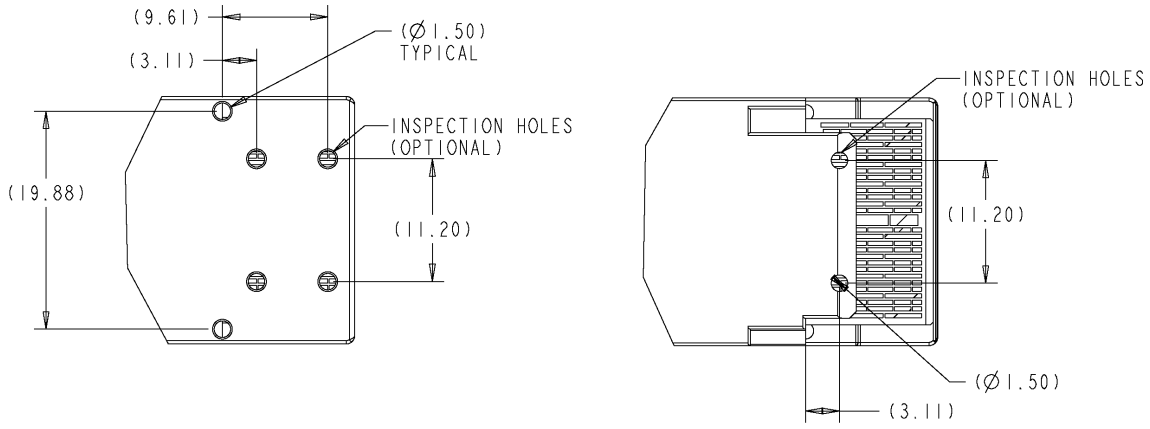


Figure 8-9: Location of inspection holes

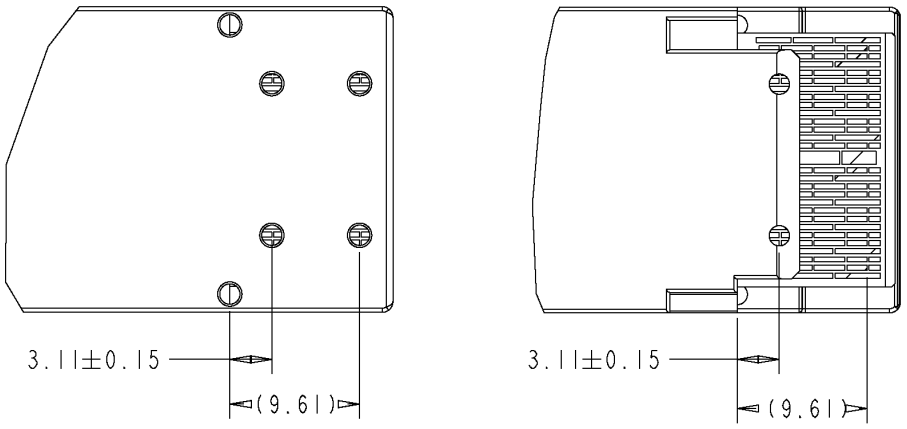


Figure 8-10: Signal pad location with respect to the forward stop

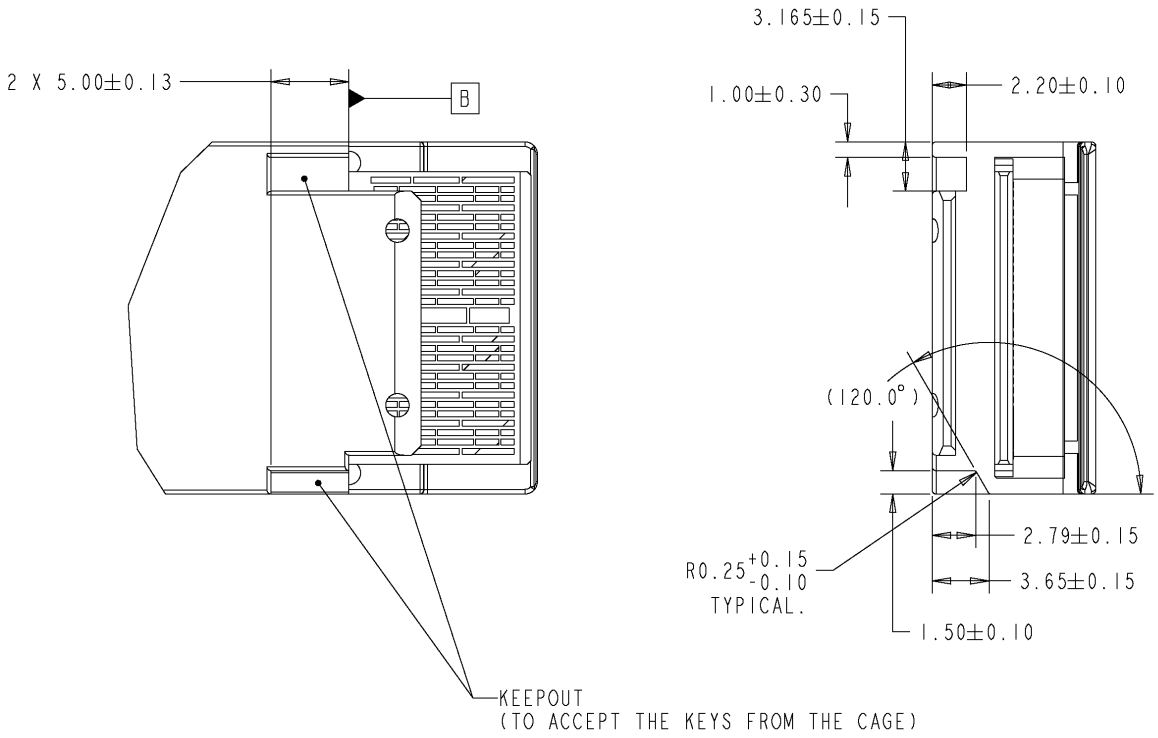


Figure 8-11: Keying feature

Module shall have a label to identify. The preferred location of the label is the bottom, and the front of the module which sticks outside of the cage as shown in the Figure 8-12.

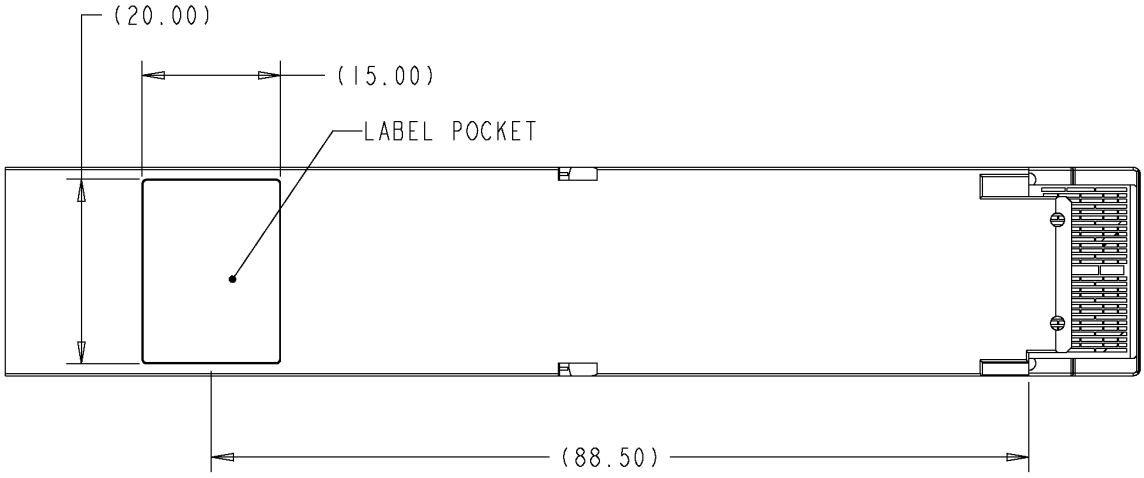


Figure 8-12: Label location (preferred)

Figure 8-13 shows the latching pocket feature of the OSFP-XD-RHS. For any dimension which is specified in OSFP-XD but not in this section, it still applies.

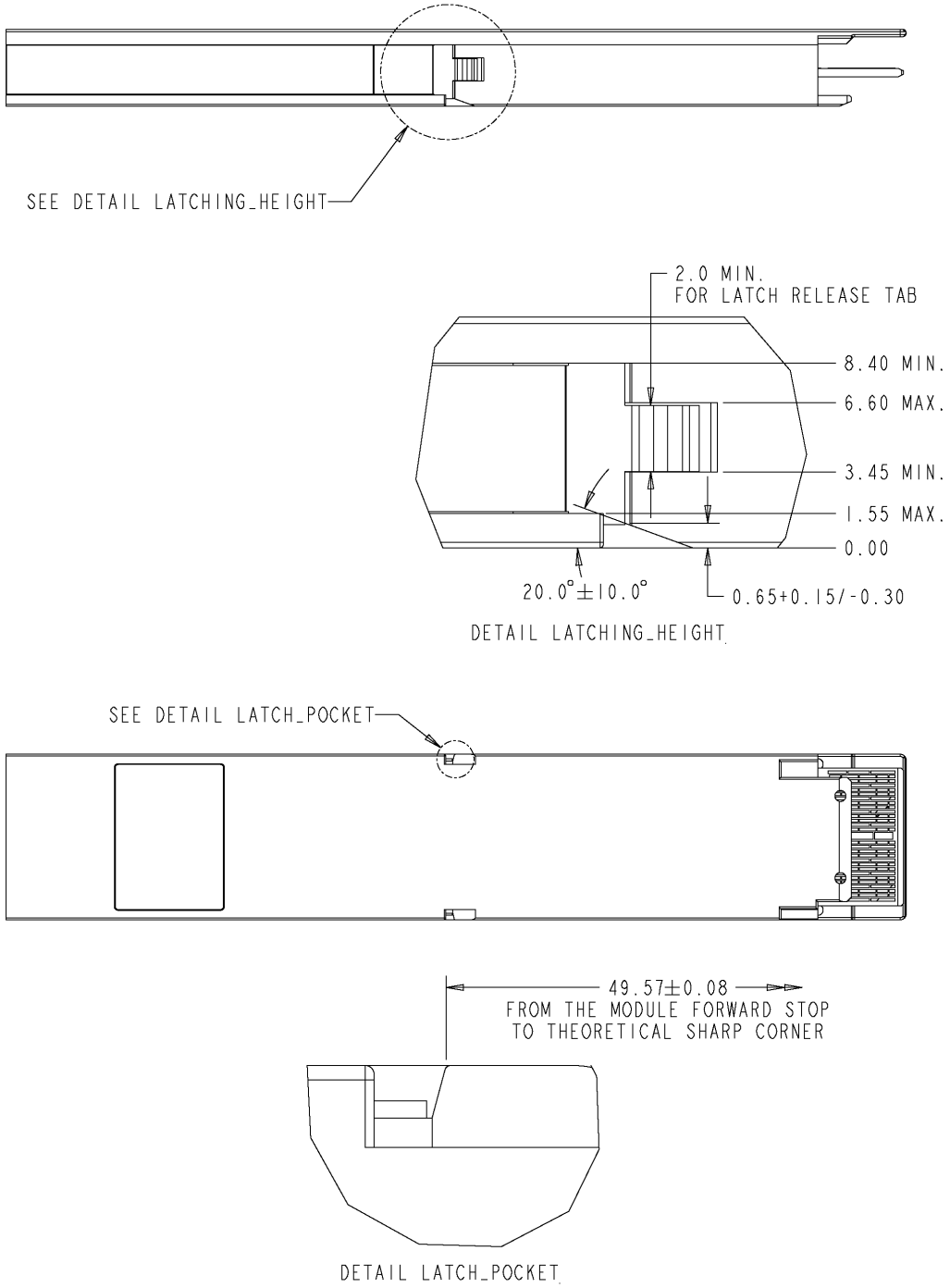


Figure 8-13: Latch pocket details of an OSFP-XD-RHS (See section 3.10 for latch cross-section)

8.3 OSFP-XD-RHS Paddle Card

Interface of the paddle card which mate with the connector of an OSFP-XD-RHS is identical with OSFP-XD.

8.4 OSFP-XD-RHS Thermal Interface Surface Requirements

The thermally conductive area of an OSFP-XD-RHS, as in the Figure 8-3, shall be compliant with specifications in Table 8-2.

Table 8-2: Surface flatness and roughness of the thermally conductive area

OSFP-XD-RHS Power (Max)	Surface Flatness	Surface Roughness
Equal or less than 5W	0.15mm or better	Ra 3.2μm or better
More than 5W	0.075mm or better	Ra 1.6μm or better
More than 14W	0.05mm or better	Ra 0.8μm or better

8.5 OSFP-XD-RHS Cage Mechanical Specification

An OSFP-XD-RHS cage has a lower height than an OSFP-XD cage and makes use of a riding heat sink for cooling. The forward stop feature in an OSFP-XD-RHS cage is shifted compared with an OSFP-XD cage to match with an OSFP-XD-RHS module. See Figure 8-16 to Figure 8-25 for the mechanical specification of the cage for OSFP-XD-RHS. The host PCB footprint is identical with OSFP-XD. Its latch feature is identical, except its geometrical reference (forward stop) has been moved.

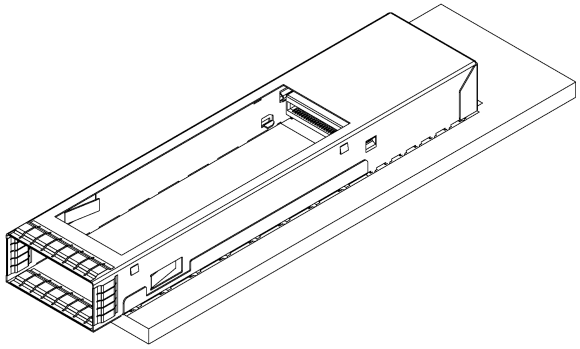


Figure 8-14: Overview of the cage and host PCB (no riding heatsink)

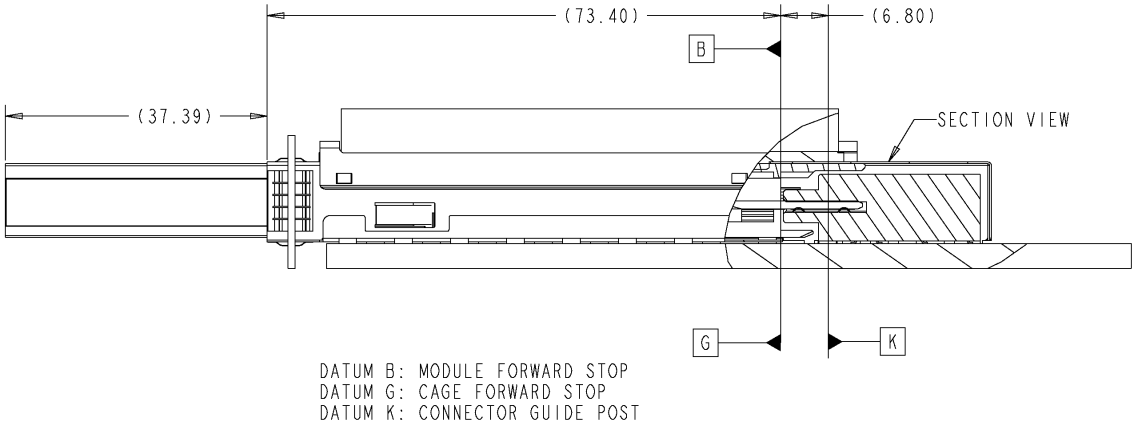


Figure 8-15: Reference dimensions with module

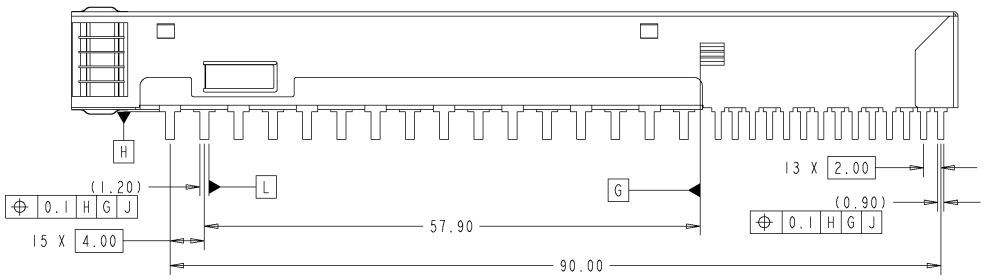


Figure 8-16: Cage positioning pins and forward stop

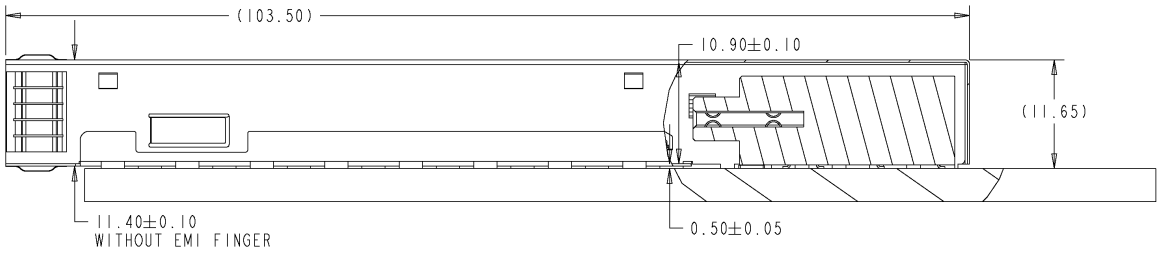


Figure 8-17: Side view of a 1x1 cage with vertical cage dimensions

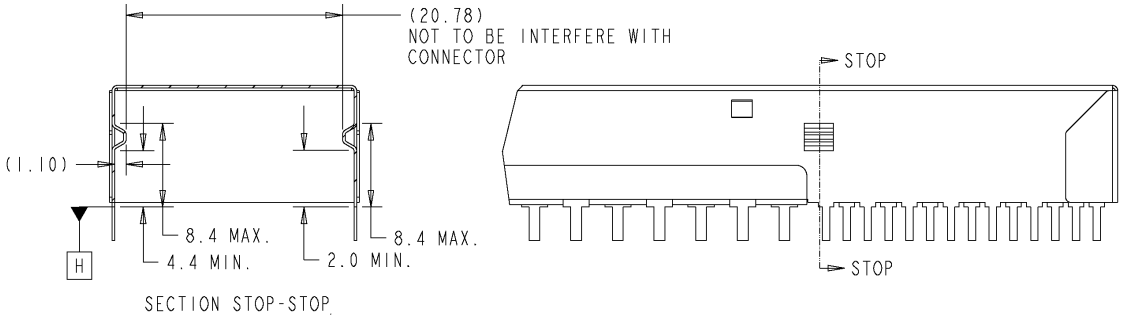


Figure 8-18: Stop feature in OSFP-XD-RHS cage

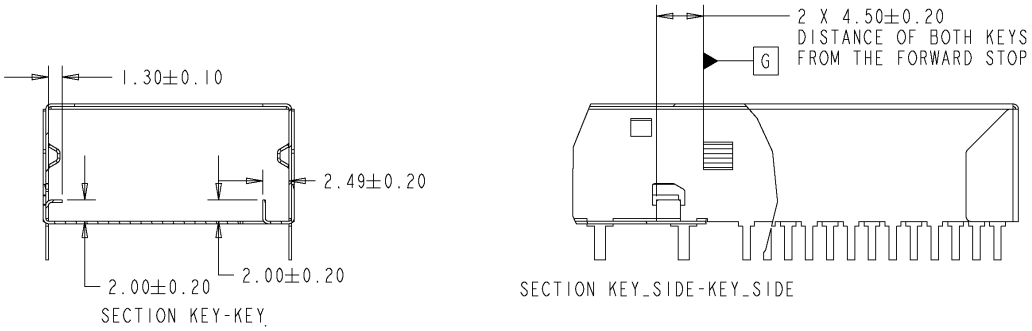


Figure 8-19: Keying feature in OSFP-XD-RHS cage

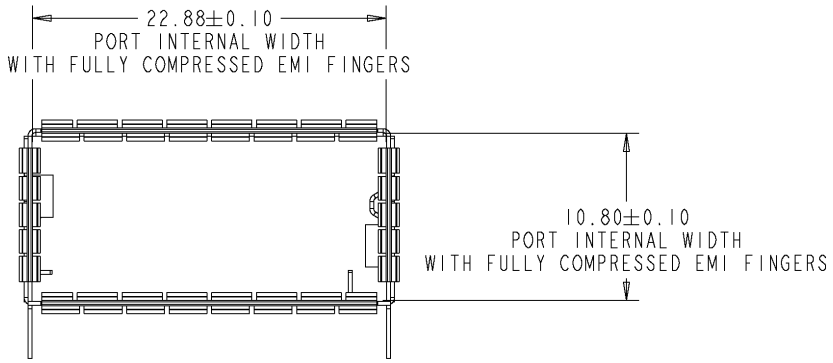


Figure 8-20: Internal width and centerline datum

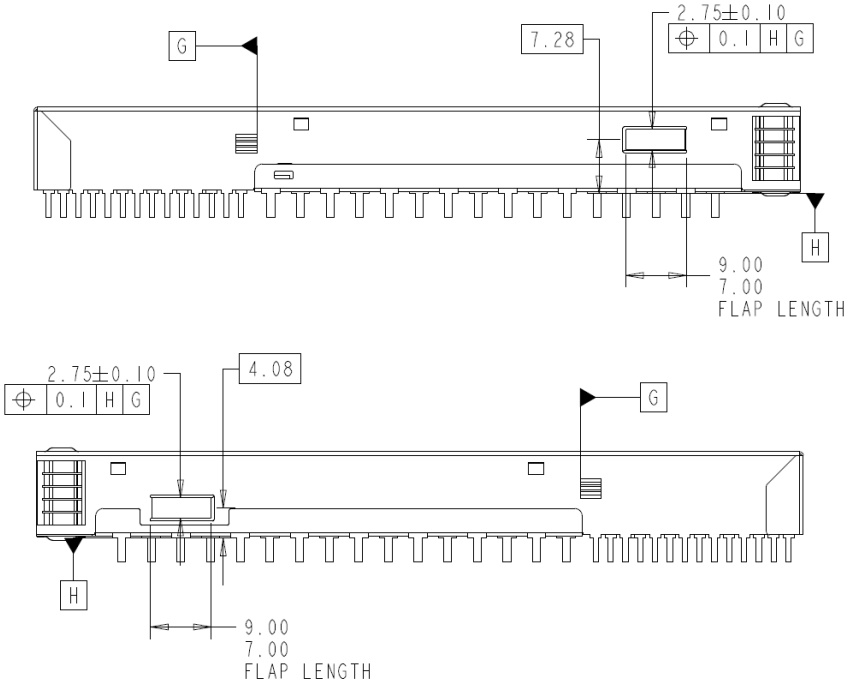


Figure 8-21: Latch feature location from bottom for OSFP-XD-RHS cage

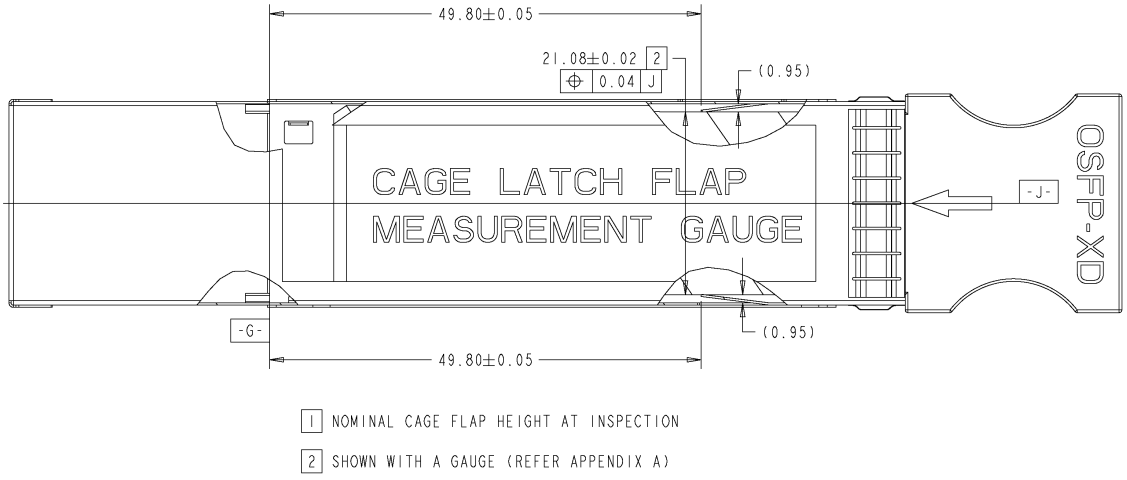


Figure 8-22: Latch feature location from stop for OSFP-XD-RHS cage

As in the Figure 4-25, the location of the latch feature (49.80±0.05mm) in the Figure 8-22 applies to the module mated condition.

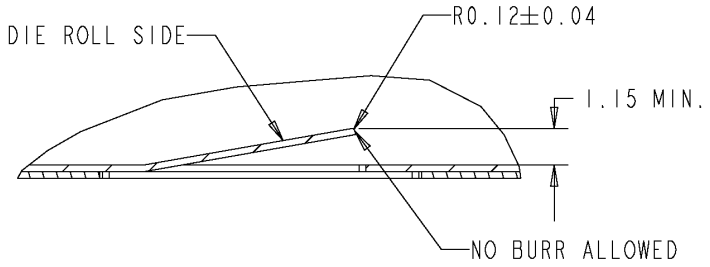


Figure 8-23: Latch feature for OSFP-XD-RHS cage

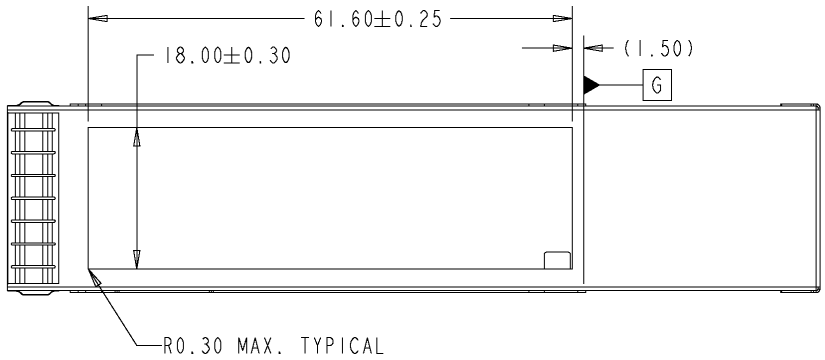


Figure 8-24: Cutout for a riding heat sink in the OSFP-XD-RHS cage

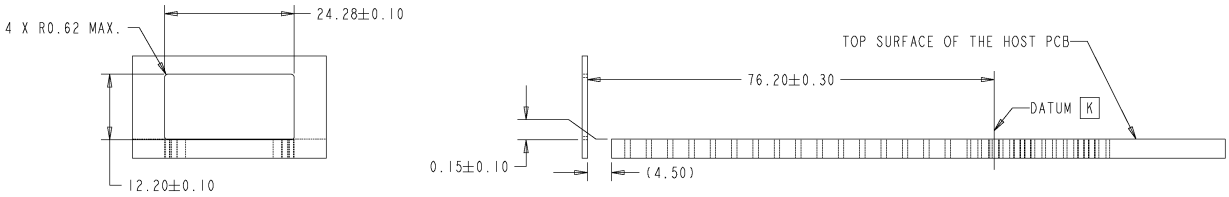


Figure 8-25: Bezel cutout for the OSFP-XD-RHS cage

A reference design for the riding heatsink leading edge and chamfer design can be found in Figure 4-15.

8.6 Maximum Heat Sink Down Force for an OSFP-XD-RHS Cage

The cage should be designed so that the force which will be applied from the riding heat sink to an OSFP-XD-RHS module shall not exceed 50N downward.

8.7 Durability of OSFP-XD-RHS

The required number of insertion and removal cycles as applicable to the OSFP-XD-RHS module and its mating connector and cage are found in Table 8-3. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 8-3: Durability of OSFP-XD-RHS

Insertion/Removal Cycles into Connector/Cage	Minimum (cycles)	Comments
Module Cycles	50	Number of cycles for an individual module, to be tested with cage, connector, and module; cage to have a riding heatsink with minimum 50N of downforce; latches may be locked out during testing
Connector/Cage Cycles	100	Number of cycles for the connector and cage with multiple modules, to be tested with cage, connector, and module; cage to have a riding heatsink with minimum 50N of downforce; latches may be locked out during testing

8.8 Custom Height OSFP-XD-RHS

There may be a custom OSFP-XD-RHS with height different than 10.5mm but otherwise having all other attributes of OSFP-XD-RHS. Details of such custom height OSFP-XD-RHS are not provided in this specification.

9 Optical PMD Block Diagrams

Below sub-sections illustrate block diagrams for a sampling of optical physical medium dependent sublayers (PMDs) that can be realized in an OSFP-XD form factor. These block diagrams are meant to serve as guidelines for better understanding of the form factor and are by no means exhaustive.

9.1 1600G PMD Block Diagrams

9.1.1 Optical PMD for 1λ SMF solution: 1600G DR16 / 1600G DR16-2

Below diagram shows 16 optical channels (32 fibers) are connected to the electrical interfaces of the OSFP-XD. Section 9.1.9 shows the detailed lane assignments for this diagram, and also for other diagrams.

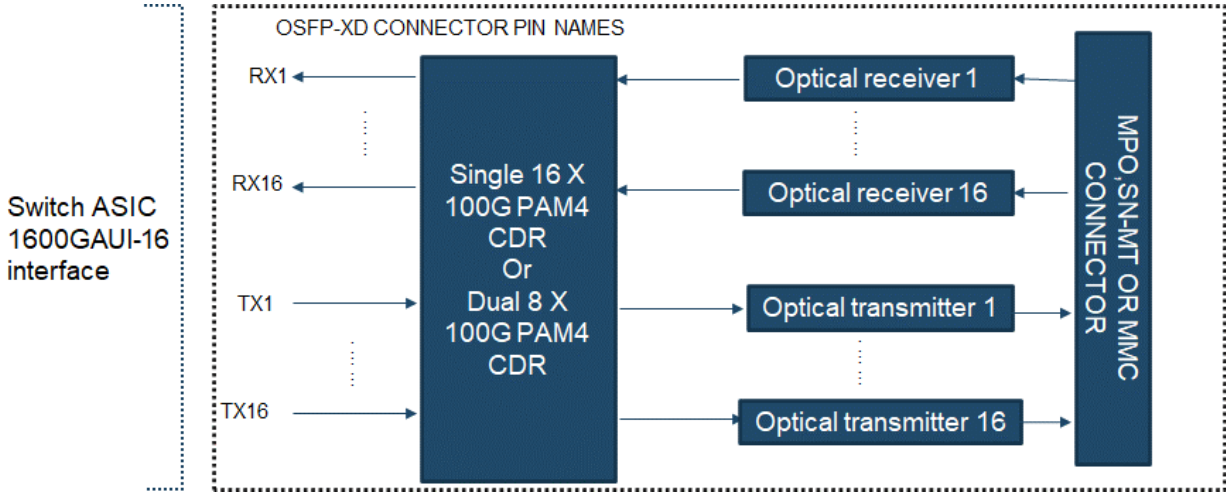


Figure 9-1: Block diagram for 1600G DR16 / 1600G DR16-2

9.1.2 Optical PMD for 1λ SMF solution: 1600G DR8 / 1600G DR8-2

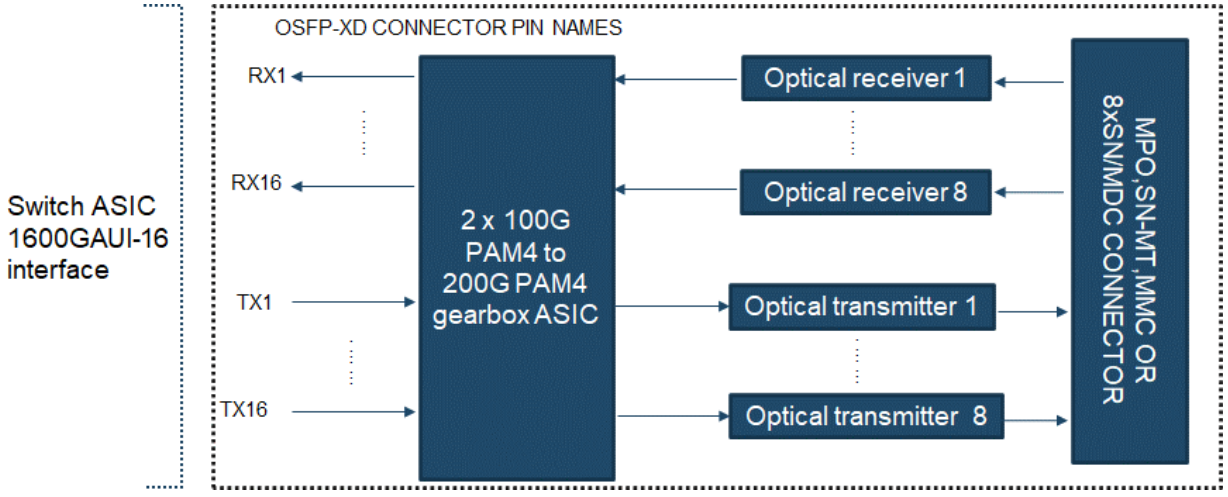


Figure 9-2: Block diagram for 1600G DR8 / 1600G DR8-2

9.1.3 Optical PMD for 2λ SMF solution: 1600G 8FR2 / 1600G 8FR2-500

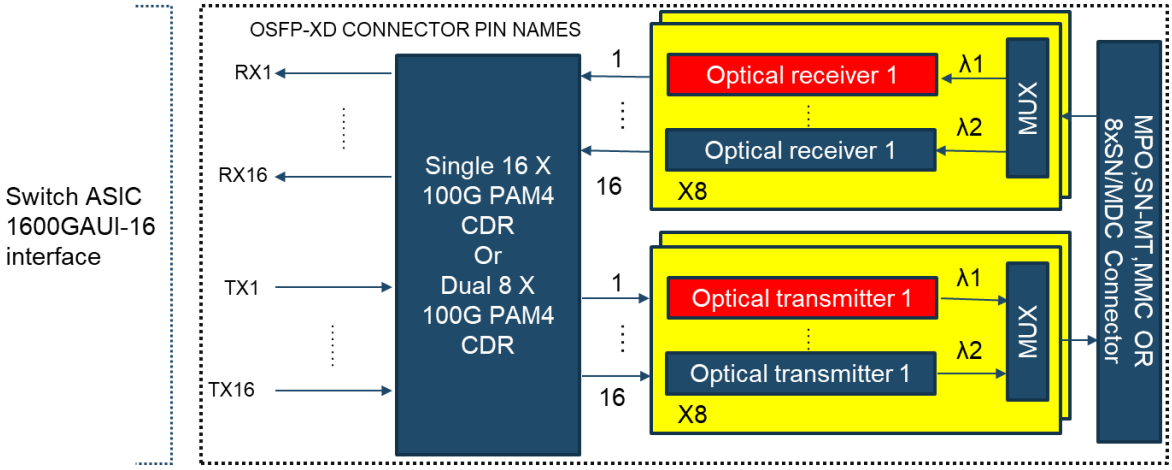


Figure 9-3: Block diagram for 1600G 8FR2 / 1600G 8FR2-500

9.1.4 Optical PMD for 2λ SMF/MMF solution: 1600G ZR2

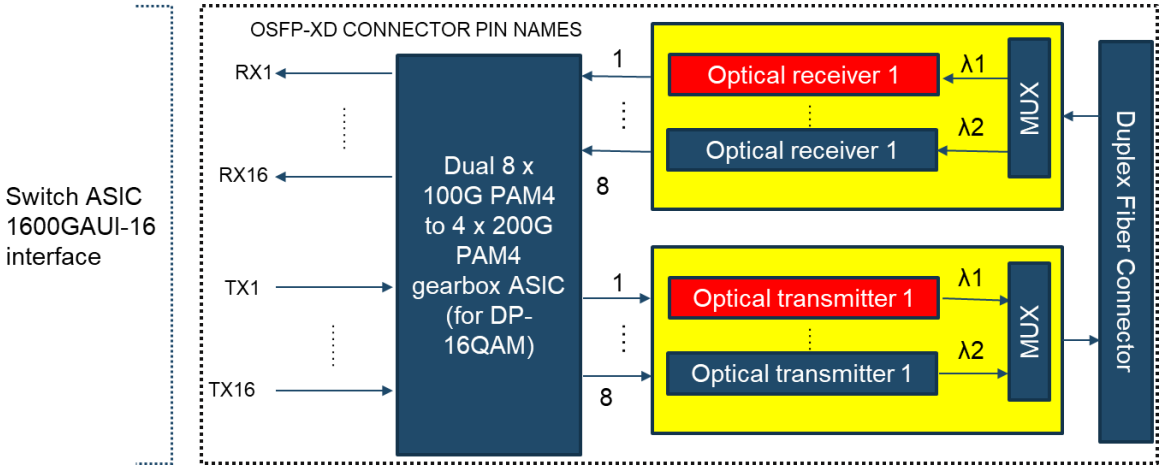


Figure 9-4: Block diagram for 1600G ZR2

9.1.5 Optical PMD for 4λ SMF solution: 1600G 4FR4 / 1600G 4FR4-500

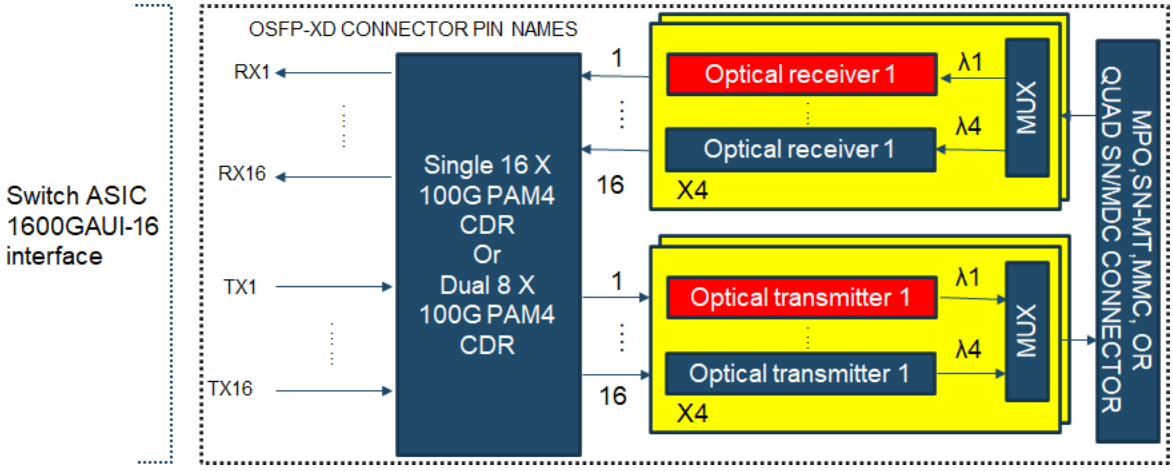


Figure 9-5: Block diagram for 1600G 4FR4 / 1600G 4FR4-500

9.1.6 Optical PMD for 4λ SMF solution: 1600G 2FR4 / 1600G 2FR4-500

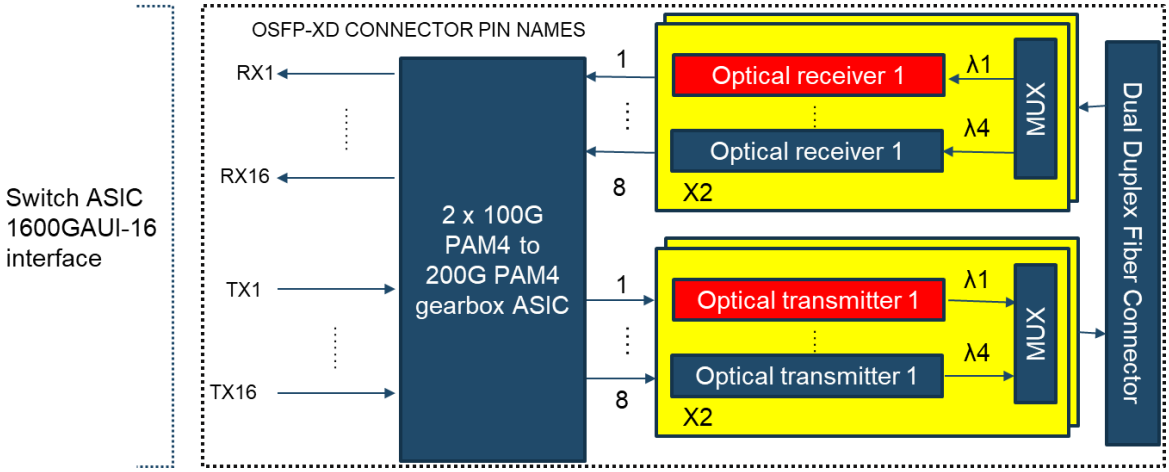


Figure 9-6: Block diagram for 1600G 2FR4 / 1600G 2FR4-500

9.1.7 Optical PMD for 8λ SMF solution: 1600G 2FR8 / 1600G 2FR8-500

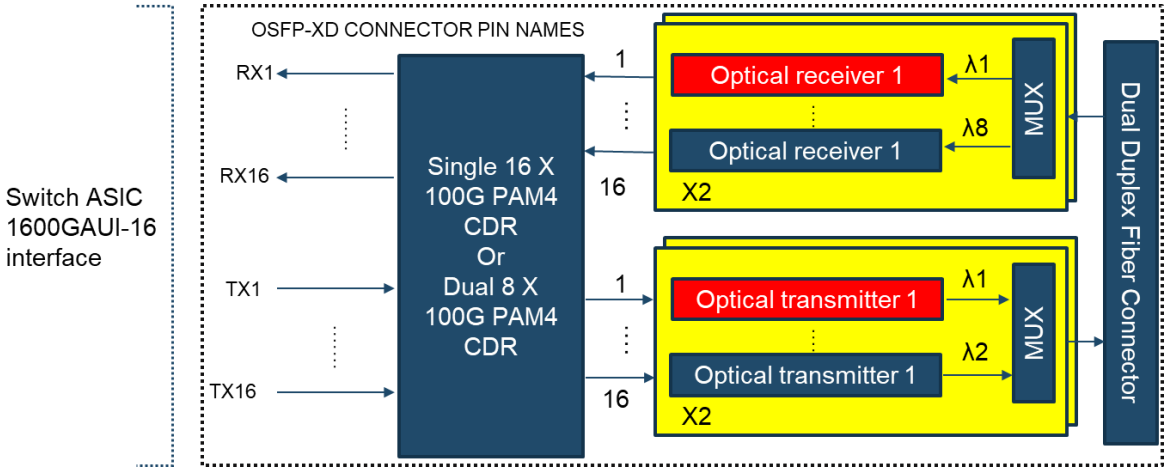


Figure 9-7: Block diagram for 1600G 2FR8 / 1600G 2FR8-500

9.1.8 Optical PMD for 8λ SMF solution: 1600G FR8 / 1600G FR8-500

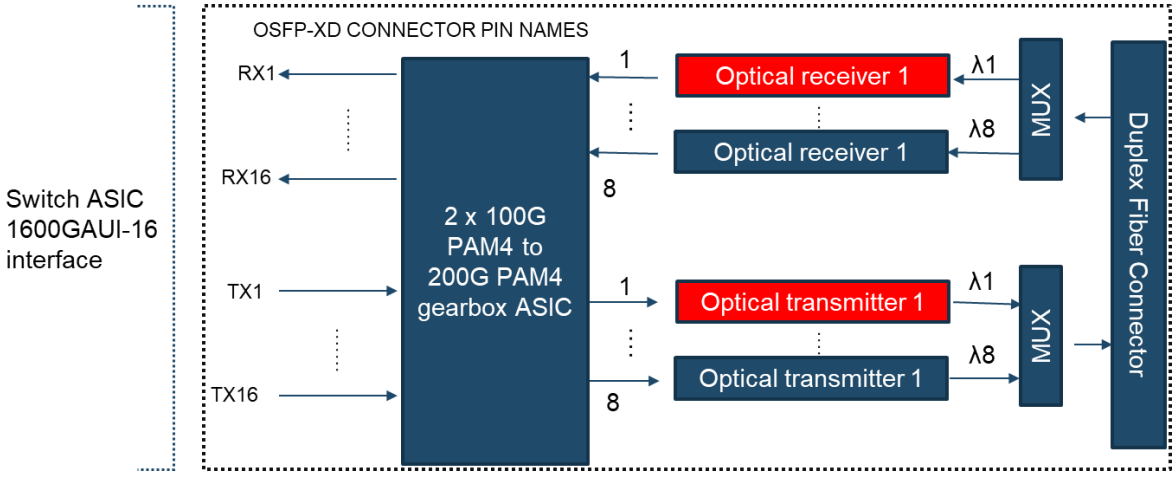


Figure 9-8: Block diagram for 1600G FR8 / 1600G FR8-500

9.1.9 Lane assignment to the electrical lanes

Table 9-1 shows the assignment of the TXs from the optical connector to the electrical lanes. RXs lanes are assigned in a same manner with TXs.

Table 9-1. Lane assignment to the electrical lanes

PMD	NOTES	Assignment of electrical lanes to Optical connector															
		TX1	TX2	TX3	TX4	TX5	TX6	TX7	TX8	TX9	TX10	TX11	TX12	TX13	TX14	TX15	TX16
DR16	16 x 1λ x 100G	TX1	TX2	TX3	TX4	TX5	TX6	TX7	TX8	TX9	TX10	TX11	TX12	TX13	TX14	TX15	TX16
DR8	8 x 1λ x 200G	TX1		TX2		TX3		TX4		TX5		TX6		TX7		TX8	
4FR2	4 x 2λ x 200G	TX1 λ1		TX1 λ2		TX2 λ1		TX2 λ2		TX3 λ1		TX3 λ2		TX4 λ1		TX4 λ2	
ZR2	1 x 2λ x 800G	TX λ1								TX λ2							
4FR4	4 x 4λ x 100G	TX1λ1	TX1λ2	TX1λ3	TX1λ4	TX2λ1	TX2λ2	TX2λ3	TX2λ4	TX3λ1	TX3λ2	TX3λ3	TX3λ4	TX4λ1	TX4λ2	TX4λ3	TX4λ4
2FR4	2 x 4λ x 200G	TX1λ1		TX1λ2		TX1λ3		TX1λ4		TX2λ1		TX2λ2		TX2λ3		TX2λ4	
2FR8	2 x 8λ x 100G	TX1λ1	TX1λ2	TX1λ3	TX1λ4	TX1λ5	TX1λ6	TX1λ7	TX1λ8	TX2λ1	TX2λ2	TX2λ3	TX2λ4	TX2λ5	TX2λ6	TX2λ7	TX2λ8
FR8	1 x 8λ x 200G	TX λ1		TX λ2		TX λ3		TX λ4		TX λ5		TX λ6		TX λ7		TX λ8	

9.2 OSFP-XD Optical Interface

Optical interfaces that can be used for the OSFP-XD modules are illustrated below. These interfaces are meant to be guideline. The centerline of the optical interfaces to be aligned with module centerline within 2mm.

The pull tab of the module should be designed so that it does not interfere with the optical plugs.

9.2.1 Duplex LC Optical Interface

Figure 9-9 shows channel orientation of the optical connector when a duplex LC connector as in IEC 61754-20 is used in an OSFP-XD module. The diagram is from the front view of a typical OSFP-XD module.

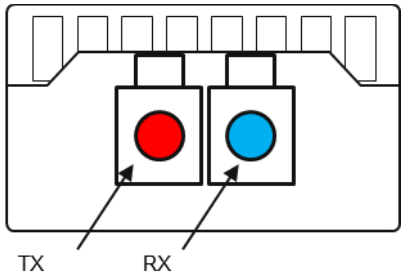


Figure 9-9: Optical receptacle and channel orientation for duplex LC connector

9.2.2 Dual Mini-LC Optical Interface

Figure *9-10* shows channel orientation of the optical connector when two Mini-LC connectors are used in side by side, consisting a dual mini-LC for an OSFP-XD module. Horizontal pitch between the mini duplex LC connectors should be 11.35mm. Note that the allowable size of the mating optical connector can be affected by the pitch of the ports on the module design and the optical connector design.

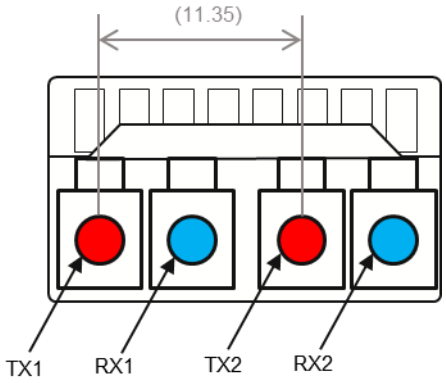


Figure 9-10*: Optical receptacle and channel orientation for Dual Mini-LC*

9.2.3 Dual Duplex LC Optical Interface

Figure 9-11 shows channel orientation of the optical connector when two duplex LC connectors are used as belly to belly, consisting of a dual duplex LC for an OSFP-XD module.

The connector should be spaced as in the Figure 9-11. Duplex LC connector with dimensions as in the Figure 9-12 will fit into this spacing.

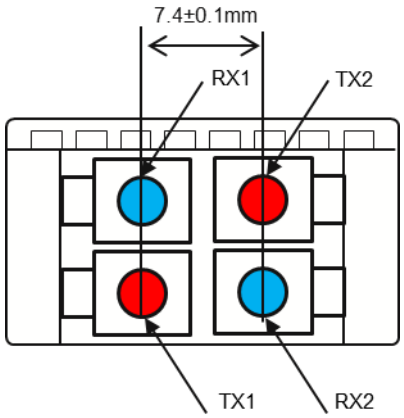


Figure 9-11: Optical receptacle and channel orientation for Dual LC

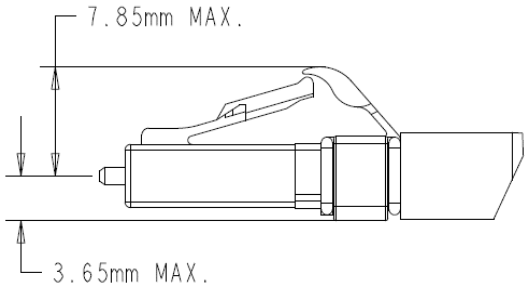


Figure 9-12: LC connector size per given belly-to-belly pitch

9.2.4 Dual CS® Optical Interface

Figure 9-13 shows channel orientation of the optical connector when a dual CS® connector is used in an OSFP-XD module.

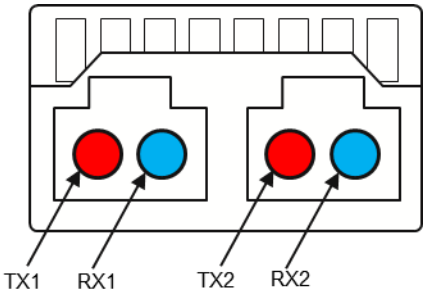


Figure 9-13: Optical receptacle and channel orientation for dual CS® connector

9.2.5 Dual MDC Optical Interface

Two MDC connectors can be used to the OSFP-XD module as in the Figure 9-14, pointing the latch of the module to the upward.

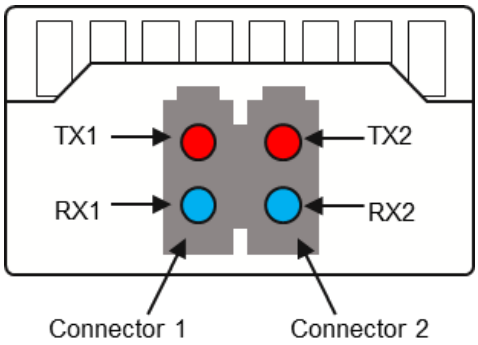


Figure 9-14: Optical receptacle for dual MDC connector (ganged)

Alternatively, two MDC connectors can be used in the OSFP-XD module as in the Figure 9-15.

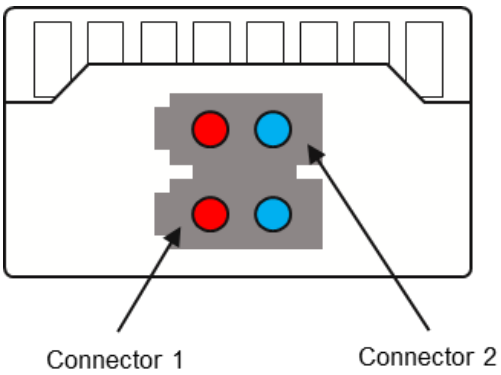


Figure 9-15: Optical receptacle for dual MDC connector (Stacked)

9.2.6 Quad MDC Optical Interface

Figure 9-16 shows channel orientation of the optical connector when a quad MDC connector is used in an OSFP-XD module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2),

receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables.

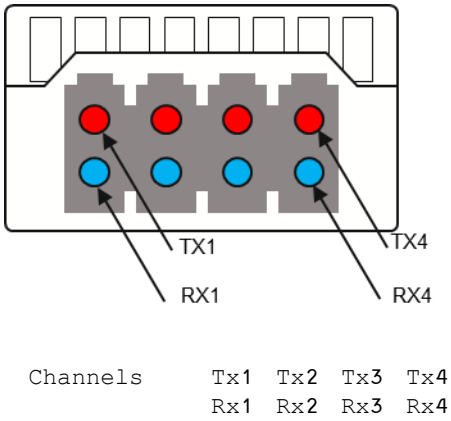


Figure 9-16: Optical receptacle and channel orientation for quad MDC connector

9.2.7 8 x MDC Optical Interface

8 MDC connectors can be placed to an OSFP-XD module as in the Figure 9-17.

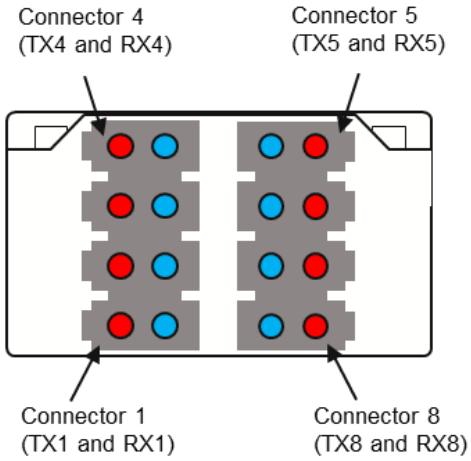


Figure 9-17: Optical receptacle and channel orientation for 8 x MDC connector

9.2.8 Dual SN Optical Interface

Two SN connectors can be used to the OSFP-XD module as in the Figure 9-18, pointing the latch of the module to the upward.

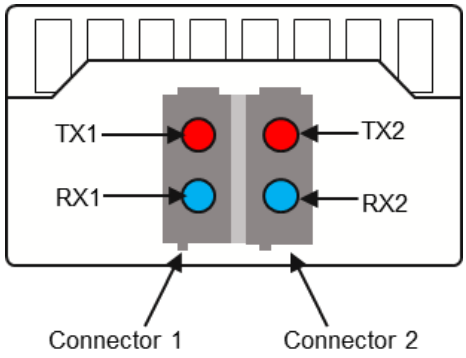


Figure 9-18: Optical receptacle for dual SN connector (ganged)

Alternatively, two SN connectors can be used in the OSFP-XD module as in the Figure 9-19.

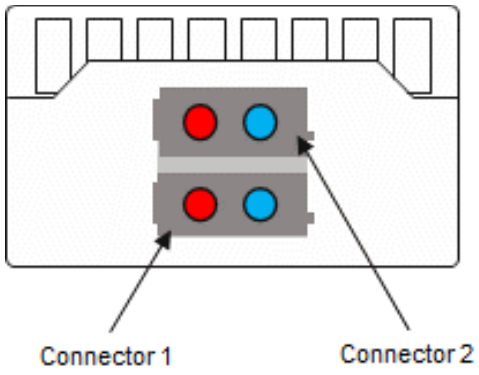
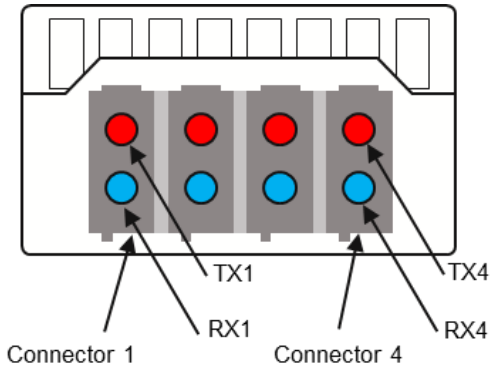


Figure 9-19: Optical receptacle for dual SN connector (Stacked)

9.2.9 Quad SN® Optical Interface

Figure 9-20 shows channel orientation of the optical connector when a quad SN® connector is used in an OSFP-XD module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2), receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables.



Channels	Tx1	Tx2	Tx3	Tx4
	Rx1	Rx2	Rx3	Rx4

Figure 9-20: Optical receptacle and channel orientation for Quad SN® connector

9.2.10 8 x SN® Optical Interface

8 SN® connectors can be placed to an OSFP-XD module as in the Figure *9-21*.

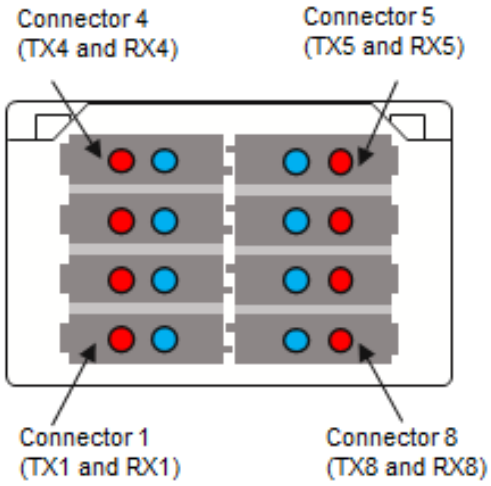
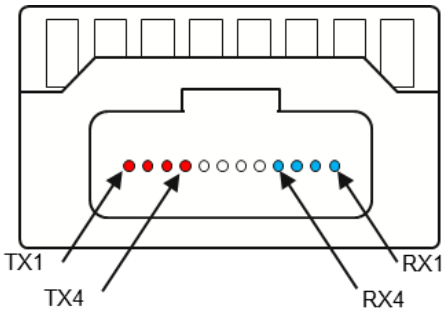


Figure 9-21: Optical receptacle and channel orientation for 8 x SN® connector

9.2.11 MPO-12 Optical Interface

Figure 9-22 shows channel orientation of the optical connector when a male MPO-12 connector as in the IEC 61754-7-1 is used in an OSFP-XD module.

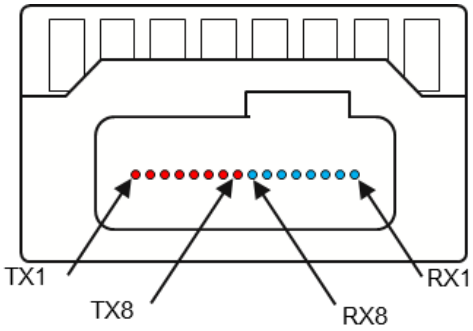



```
Channels                Tx1 Tx2 Tx3 Tx4 x x x x Rx4 Rx3 Rx2 Rx1
(x: unused position)
```

Figure 9-22: Optical receptacle and channel orientation for MPO-12 connector

9.2.12 MPO-16 Optical Interface

Figure 9-23 shows channel orientation of the optical connector when a male MPO-16 connector as in the TIA-604-18 is used in an OSFP-XD module.

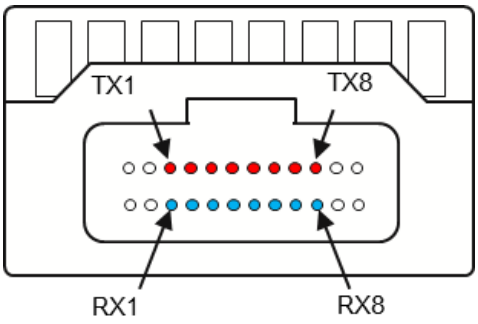


Channels	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1

Figure 9-23: Optical receptacle and channel orientation for MPO-16 connector

9.2.13 MPO-12 Two Row Optical Interface

Figure 9-24 shows channel orientation of the optical connector when a male MPO-12 Two Row connector as in the TIA-604-18 is used in an OSFP-XD module.



Channels	x	x	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	x	x
(x: unused position)	x	x	Rx1	Rx2	Rx3	Rx4	Rx5	Rx6	Rx7	Rx8	x	x

Figure 9-24: Optical receptacle and channel orientation for MPO-12 Two Row connector

9.2.14 Dual MPO Optical Interface

Figure 9-25 shows channel orientation of the optical connector when dual MPO-12 connectors are used in an OSFP-XD module. MPO-12 connectors, which channel assignment within the connector to be as in the Figure 9-22, will be used as depicted in the figure.

Figure 9-25 also shows the spacing between the connectors. Figure 9-26 shows MPO connector shows the size of the allowable connector in the given pitch.

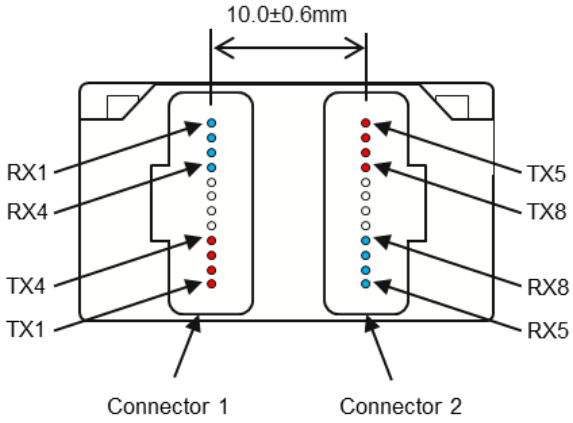


Figure 9-25: Optical receptacle and channel orientation for Dual MPO connector

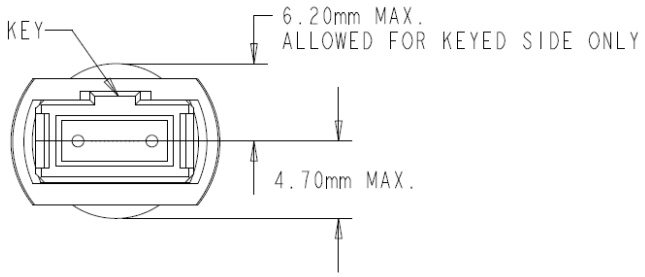


Figure 9-26: MPO connector size per given belly-to-belly pitch

9.2.15 MMC Optical Interface

Figure 9-27 shows the diagram when a single MMC connector with 24 (2x12) or 32 (2x16) fibers is used on the OSFP-XD module.

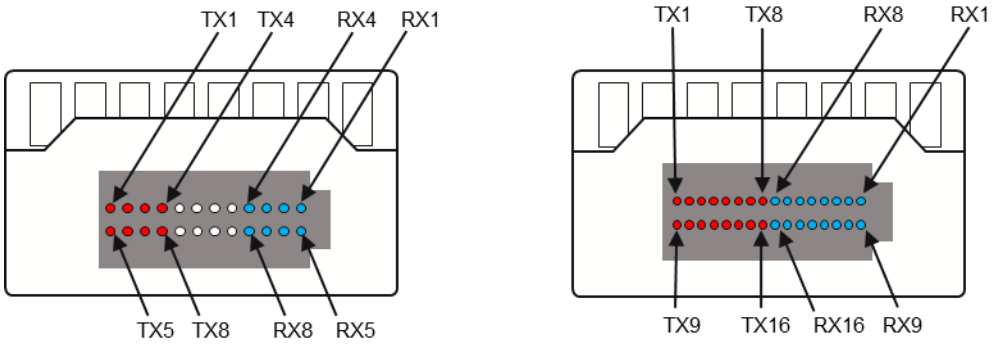


Figure 9-27: Optical receptacle for MMC connector (2x12 and 2x16 fibers)

9.2.16 Dual MMC Optical Interface

Figure 9-28 and Figure 9-29 show the diagram when two MMC connectors with 12 or 16 fibers are implemented in the OSFP-XD module. Lane assignments in the ferrule are in a same manner with MPO.

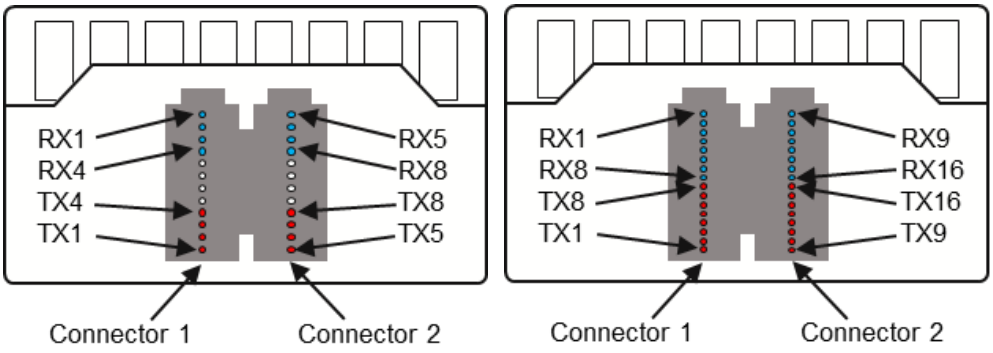


Figure 9-28: Optical receptacle for dual MMC connector (Ganged)

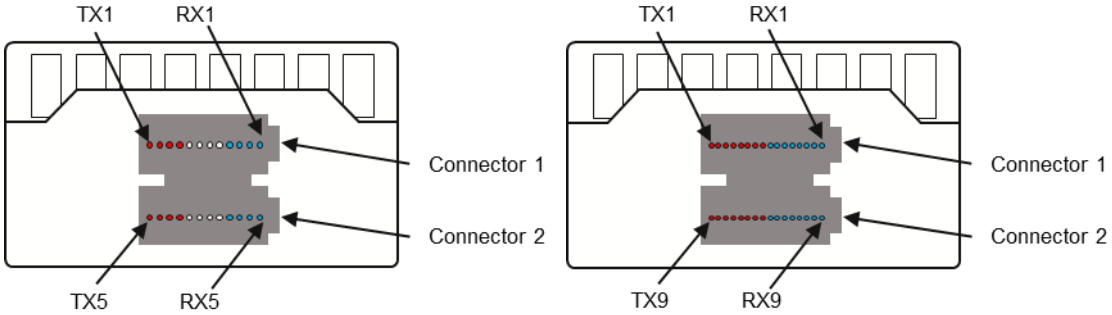


Figure 9-29: Optical receptacle for dual MMC connector (Stacked)

9.2.17 SN-MT Optical Interface

Figure 9-30 shows the diagram when a single SN-MT connector is used. In the shown case, 24 (2x12) or 32 fibers (2x16) are used.

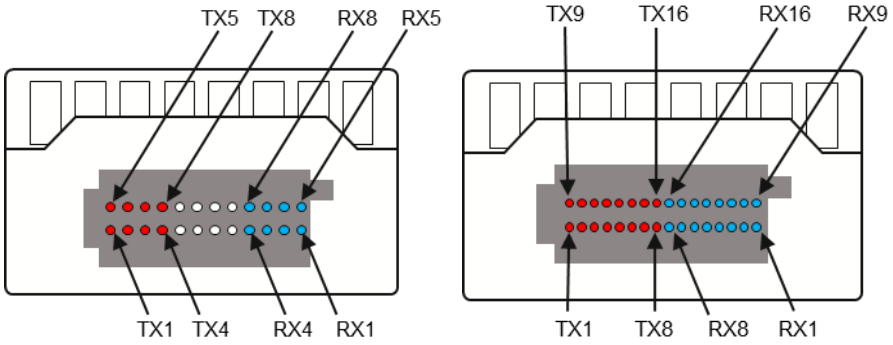


Figure 9-30: Optical receptacle for SN-MT connector (2x16 fibers)

9.2.18 Dual SN-MT Optical Interface

Figure 9-31 and Figure 9-32 show the diagram when two SN-MT connectors with 12 or 16 fibers are implemented in the OSFP-XD module.

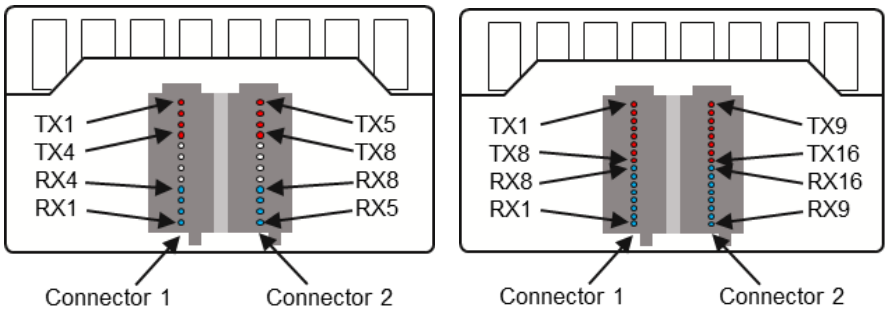


Figure 9-31: Optical receptacle for dual SN-MT connector (Ganged)

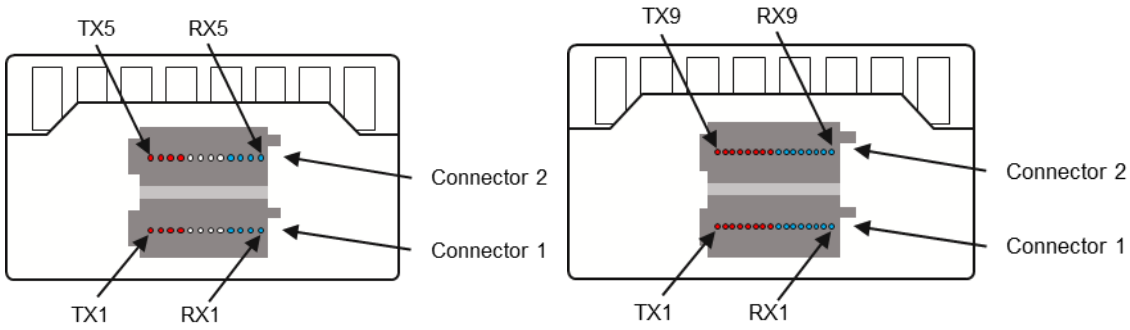


Figure 9-32: Optical receptacle for dual SN-MT connector (Stacked)

9.2.19 MXC Optical Interface

Figure 9-33 shows channel orientation of a MXC connector with 16 fibers when it is used in the OSFP-XD module.

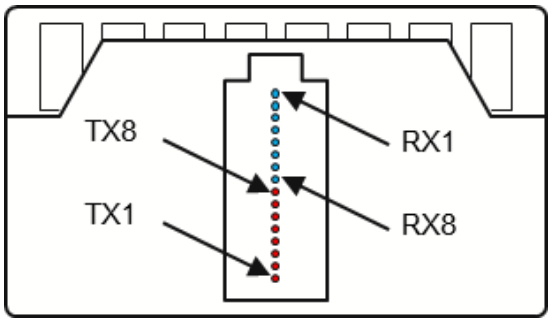


Figure 9-33: Optical receptacle and channel orientation for MXC connector

9.2.20 Dual MXC Optical Interface

Figure 9-34 shows channel orientation of the optical connector when dual MXC connectors are used in an OSFP-XD module. Connector 1 will be used for the first half of the channels of the module (TX1~8 and RX 8~1) while the Connector 2 will be used for the second half of the channels of the module (TX9~16 and RX16~9).

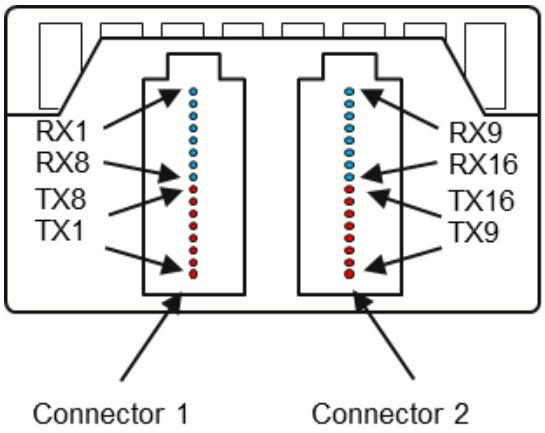


Figure 9-34: Optical receptacle and channel orientation for Dual MXC connector

10 Electrical Interface

10.1 Module Electrical Connector

The electrical interface of an OSFP-XD module consists of a 120 contacts edge connector as illustrated by the diagram in Figure 10-1. It provides 32 contacts for 16 differential pairs of high-speed transmit signals, 32 contacts for 16 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 8 contacts for power, 40 contacts for ground, and 4 contacts designated as application/vendor specific.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

The chassis ground (case common) of the OSFP-XD module shall be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module. When an OSFP-XD module is not installed, the signals to the connector within the unused cage should be disabled to minimize electromagnetic interference (EMI) emissions.

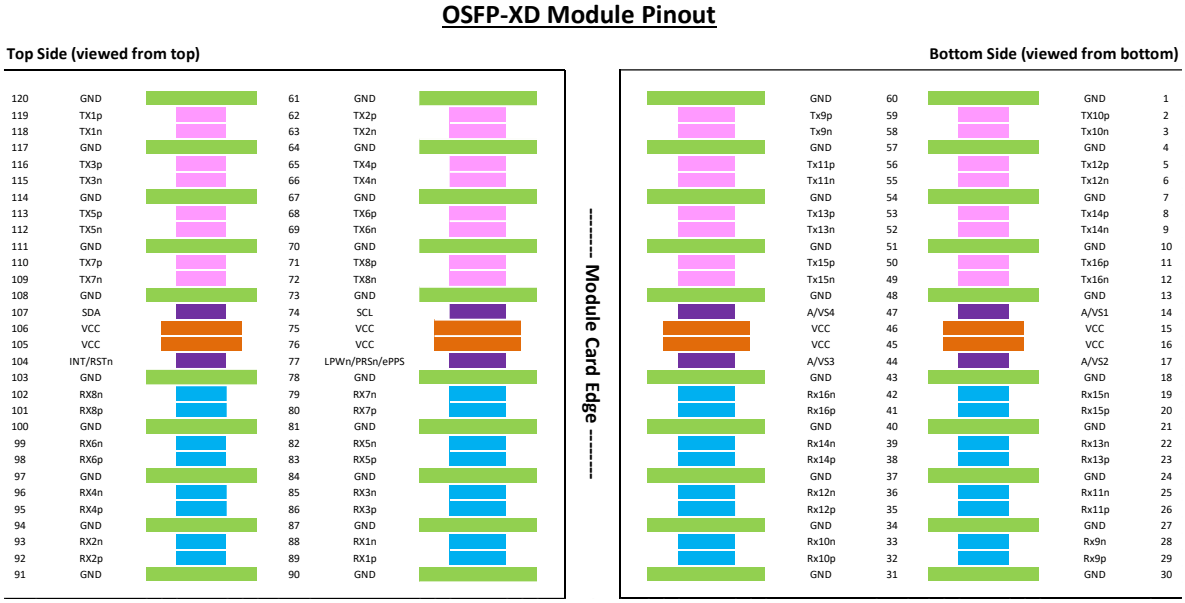


Figure 10-1: OSFP-XD module pinout

10.2 Pin Descriptions

Table 10-1: OSFP-XD module signal pin descriptions

Name	Direction	Description
TX[16:1]p	input	Transmit differential pairs from host to module.
TX[16:1]n	input	
RX[16:1]p	output	Receive differential pairs from module to host.
RX[16:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn/ePPS	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 10.5.3 There is also optional support for an ePPS PTP clock or reference clock input as described in Section 10.5.4
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 10.5.2
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.
A/VS[4:1]	-	Application/Vendor Specific signals as described in Section 10.5.5

10.3 Pin List

Table 10-2: OSFP-XD connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX10p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX10n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX12p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX12n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX14p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX14n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX16p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX16n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	A/VS1	Application/Vendor Specific	-	-	3	See Section 10.5.5
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	A/VS2	Application/Vendor Specific	-	-	3	See Section 10.5.5
18	GND	Ground			1	
19	RX15n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX15p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX13n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX13p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX11n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX11p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
27	GND	Ground			1	
28	RX9n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX9p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX10p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX10n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX12p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX12n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX14p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX14n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX16p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX16n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	A/VS3	Application/Vendor Specific	-	-	3	See Section 10.5.5
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	A/VS4	Application/Vendor Specific	-	-	3	See Section 10.5.5
48	GND	Ground			1	
49	TX15n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX15p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX13n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX13p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX11n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX11p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX9n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX9p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	
61	GND	Ground			1	
62	Tx2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
63	Tx2n	Transmitter Data Inverted	CML-I	Input from Host	3	
64	GND	Ground			1	
65	Tx4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
66	Tx4n	Transmitter Data Inverted	CML-I	Input from Host	3	
67	GND	Ground			1	
68	Tx6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
69	Tx6n	Transmitter Data Inverted	CML-I	Input from Host	3	
70	GND	Ground			1	
71	Tx8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
72	Tx8n	Transmitter Data Inverted	CML-I	Input from Host	3	
73	GND	Ground			1	
74	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
75	VCC	+3.3V Power		Power from Host	2	
76	VCC	+3.3V Power		Power from Host	2	
77	LPWn/PRSn/ePPS	Low-Power Mode / Module Present / ePPS PTP Clock (optional)	Multi-Level	Bi-directional	3	See pin description for required circuit
78	GND	Ground			1	
79	Rx7n	Receiver Data Inverted	CML-O	Output to Host	3	
80	Rx7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
81	GND	Ground			1	
82	Rx5n	Receiver Data Inverted	CML-O	Output to Host	3	
83	Rx5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
84	GND	Ground			1	
85	Rx3n	Receiver Data Inverted	CML-O	Output to Host	3	
86	Rx3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
87	GND	Ground			1	
88	Rx1n	Receiver Data Inverted	CML-O	Output to Host	3	
89	Rx1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
90	GND	Ground			1	
91	GND	Ground			1	
92	Rx2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
93	Rx2n	Receiver Data Inverted	CML-O	Output to Host	3	
94	GND	Ground			1	
95	Rx4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
96	Rx4n	Receiver Data Inverted	CML-O	Output to Host	3	
97	GND	Ground			1	
98	Rx6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
99	Rx6n	Receiver Data Inverted	CML-O	Output to Host	3	
100	GND	Ground			1	
101	Rx8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
102	Rx8n	Receiver Data Inverted	CML-O	Output to Host	3	
103	GND	Ground			1	
104	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
105	VCC	+3.3V Power		Power from Host	2	
106	VCC	+3.3V Power		Power from Host	2	
107	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
108	GND	Ground			1	
109	Tx7n	Transmitter Data Inverted	CML-I	Input from Host	3	
110	Tx7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
111	GND	Ground			1	
112	Tx5n	Transmitter Data Inverted	CML-I	Input from Host	3	
113	Tx5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
114	GND	Ground			1	
115	Tx3n	Transmitter Data Inverted	CML-I	Input from Host	3	
116	Tx3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
117	GND	Ground			1	
118	Tx1n	Transmitter Data Inverted	CML-I	Input from Host	3	
119	Tx1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
120	GND	Ground			1	

10.4 High-Speed Signals

A fully-populated OSFP-XD solution consists of 16 transmit and 16 receive differential pairs identified as TX[16:1]p / TX[16:1]n and RX[16:1]p / RX[16:1]n. These signals can be operated in port configurations of either a single 16-lanes, dual 8-lanes, quad 4-lanes or 16 individual lanes depending on the capability of the host ASIC.

3.2TAUI-16 mode provides 16 differential lanes using 224G-PAM4 signaling operating at 106.25 GBaud. This results in 16 lanes of 200Gb/s for a total of 3.2Tb/s. This mode allows connection to PMD configurations of 2x1.6T, 4x800G, 8x400G, and 16x200G.

1.6TAUI-16 mode provides 16 differential lanes using 112G-PAM4 signaling operating at 53.125 GBaud. This results in 16 lanes of 100Gb/s for a total of 1.6Tb/s. This mode allows connection to PMD configurations of 1x1.6T, 2x800G, 4x400G, 8x200G, and 16x100G.

The lane assignments for a fully-populated OSFP-XD solution shown in Table 10-3 shall be used for the different PMD configurations.

The OSFP-XD module also has the capability to support a half-populated solution (“XD-8”). The high-speed signals consists of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in port configurations of either a single 8-lanes, dual 4-lanes, quad 2-lanes or 8 individual lanes depending on the capability of the host ASIC.

1.6TAUI-8 mode provides 8 differential lanes using 224G-PAM4 signaling operating at 106.25 GBaud. This results in 8 lanes of 200Gb/s for a total of 1.6Tb/s. This mode allows connection to PMD configurations of 1x1.6T, 2x800G, 4x400G, 8x200G.

800GAUI-8 mode provides 8 differential lanes using 112G-PAM4 signaling operating at 53.125 GBaud. This results in 8 lanes of 100Gb/s for a total of 800Gb/s. This mode allows connection to PMD configurations of 1x800G, 2x400G, 4x200G or 8x100G.

The lane assignments for a half-populated OSFP-XD solution (“XD-8”) shown in Table 10-4 shall be used for the different PMD configurations.

In all configurations, the high-speed signals follow the electrical specifications of IEEE802.3df, IEEE802.3dj, and IEEE802.3ck.

Table 10-3: High-speed signal lane mapping

(*L means Lane, L1 means Lane 1 in the port.)
(**P means Port, P1 means Port 1 in the PMD configuration)

PMD Configuration	Transmit and Receive Lane Assignments															
	L1*	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**	**L9**	**L10**	**L11**	**L12**	**L13**	**L14**	**L15**	**L16**
1x1.6T (112G-PAM4)	P1**															
2x1.6T (224G-PAM4) 2x800G (112G-PAM4)	P1								P2							
	L1	L2	L3	L4	L5	L6	L7	L8	L1	L2	L3	L4	L5	L6	L7	L8
4x800G (224G-PAM4) 4x400G (112G-PAM4)	P1				P2				P3				P4			
	L1	L2	L3	L4	L1	L2	L3	L4	L1	L2	L3	L4	L1	L2	L3	L4
8x400G (224G-PAM4) 8x200G (112G-PAM4)	P1		P2		P3		P4		P5		P6		P7		P8	
	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
16x200G (224G-PAM4) 16x100G (112G-PAM4)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16

Table 10-4: High-speed signal lane mapping

(*L means Lane, L1 means Lane 1 in the port.)
(**P means Port, P1 means Port 1 in the PMD configuration)

PMD Configuration	Transmit and Receive Lane Assignments															
	L1*	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**	**L9**	**L10**	**L11**	**L12**	**L13**	**L14**	**L15**	**L16**
1x1.6T (224G-PAM4) 1x800G (112G-PAM4)	P1								Not Used							
	L1	L2	L3	L4	L5	L6	L7	L8								
2x400G (224G-PAM4) 2x200G (112G-PAM4)	P1				P2				Not Used							
	L1	L2	L3	L4	L1	L2	L3	L4								
4x400G (224G-PAM4) 4x200G (112G-PAM4)	P1		P2		P3		P4		Not Used							
	L1	L2	L1	L2	L1	L2	L1	L2								
8x200G (224G-PAM4) 8x100G (112G-PAM4)	P1	P2	P3	P4	P5	P6	P7	P8	Not Used							

10.5 Low-Speed Signals

There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn/ePPS and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals. LPWn/PRSn/ePPS and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

10.5.1 SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I^2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I^2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I^2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- Optional - I3C Single Data Rate (SDR) ≤ 12.5 Mbit/s

The host shall default to using 100 kbit/s standard-mode I^2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP-XD, the host may then use I^2C Fast-mode, I^2C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I^2C-bus specification or Single Data Rate mode as defined in the Specification for I3C.

10.5.2 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 10-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-high signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 10-2 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INT signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

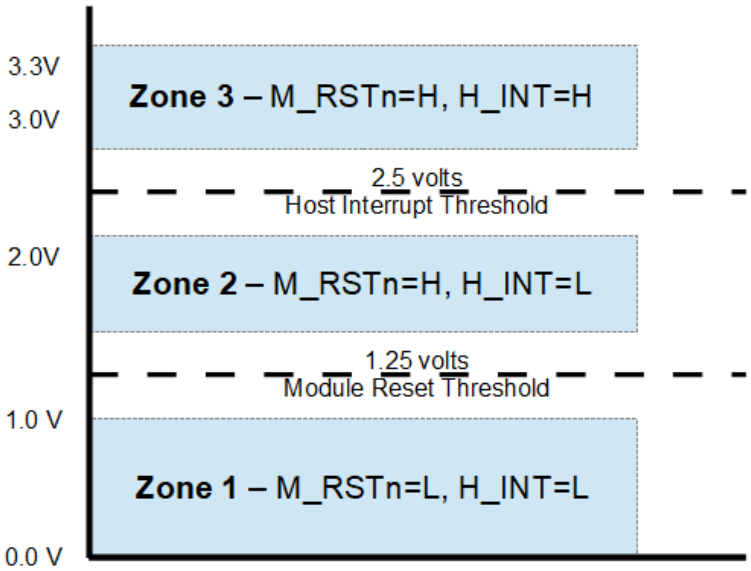


Figure 10-2: INT/RSTn voltage zones

- Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INT=Low). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 10-5.
- Zone 2 – Normal operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INT=Low). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 10-5.
- Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INT=High). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 10-5.

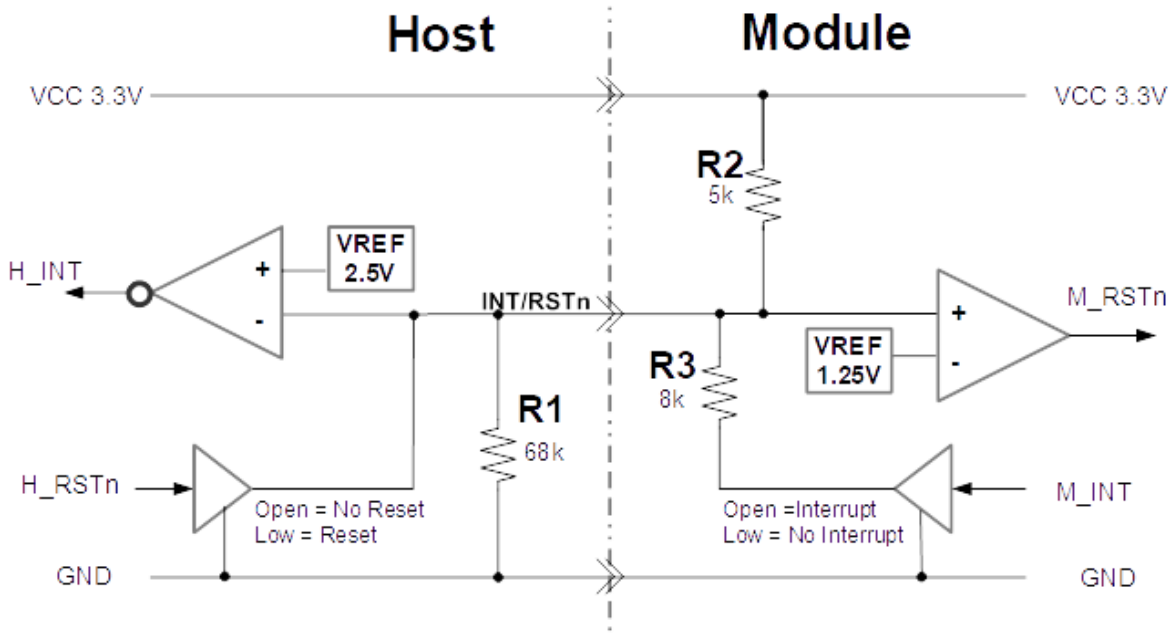


Figure 10-3: INT/RSTn circuit

Table 10-5: INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INT	2.500	2.475	2.525	Volts	Precision voltage reference for H_INT
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

10.5.3 LPWn/PRSn/ePPS

LPWn/PRSn/ePPS is a dual function signal that allows two different modes of operation.

The primary mode is consistent with the OSFP MSA and supports LPWn/PRSn which allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 10-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The secondary (optional) mode supports PRSn/ePPS which allows the host to provide an ePPS clock to the module and the module to indicate Module Present. The circuits show in Figure 10-6 or Figure 10-7 show how to support ePPS. Figure 10-6 provides the ability for the host to support either LPWn/PRSn or PRSn/ePPS modes while Figure 10-7 is specific to PRSn/ePPS mode.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 10-4 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

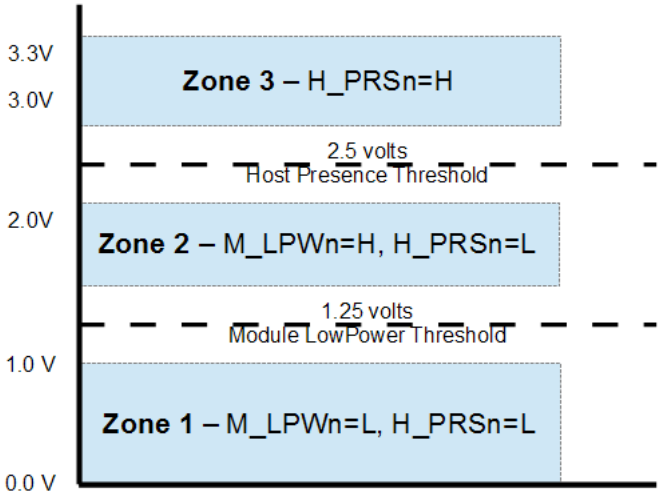


Figure 10-4: LPWn/PRSn voltage zones

- Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 10-6.
- Zone 2 – High Power mode – Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 10-6.
- Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 10-6.

Module Removal – If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the module shall assert Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and

disable transmitters within the time specified by T_hplp in Table 10-14. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level then 3.3V LVCMOS is preferred.

For very low cost modules, such as DAC, the voltage comparator on the module may be omitted and the LPWn/PRSn pin shall in that case be tied to GND in the module. This type of module may only be used for low power mode (Power Class 1).

The module transmitters must be disabled when in Low Power mode. This ensures Power Class 1 and also provides a fast hardware shut down mechanism for applications such as redundancy switch-over. In addition, software controlled transmitter disable is provided by the TX Disable register via the I^2C interface.

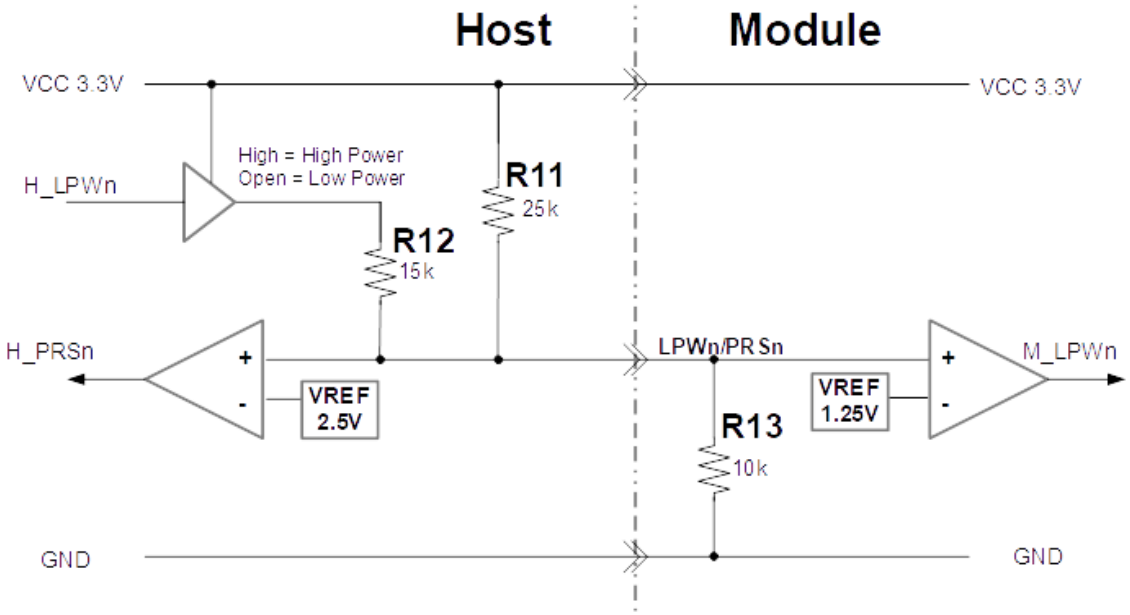


Figure 10-5: LPWn/PRSn circuit

Table 10-6: LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

10.5.4 ePPS/Clock PTP Reference Clock (Optional)

Support for ePPS/Clock can be enabled with additional circuitry on the LPWn/PRSn signal. The circuit shown in Figure 10-6 enables an superposition of an ePPS/Clock to be transmitted from the Host to the Module without compromising the LPWn/PRSn functionality detailed in Section 10.5.3. When a capable module is recognized, the host can enable a clock signal to be transmitted on the dual function LPWn/PRSn signal while operating in Zone 2, or High Power Mode. The clock driver is controlled by the signal H_CLK_ON, an active-high signal, and must be de-asserted when the host recognizes that a legacy module is plugged in that does not support ePPS/Clock mode. The recommended voltage swing is CML single-ended (min) to LVCMOS (max). The host may have to set the module receiver input to the CLK logic type. The process would be detailed in a future release of CMIS, and is currently not defined in CMIS Revision 5.2 .

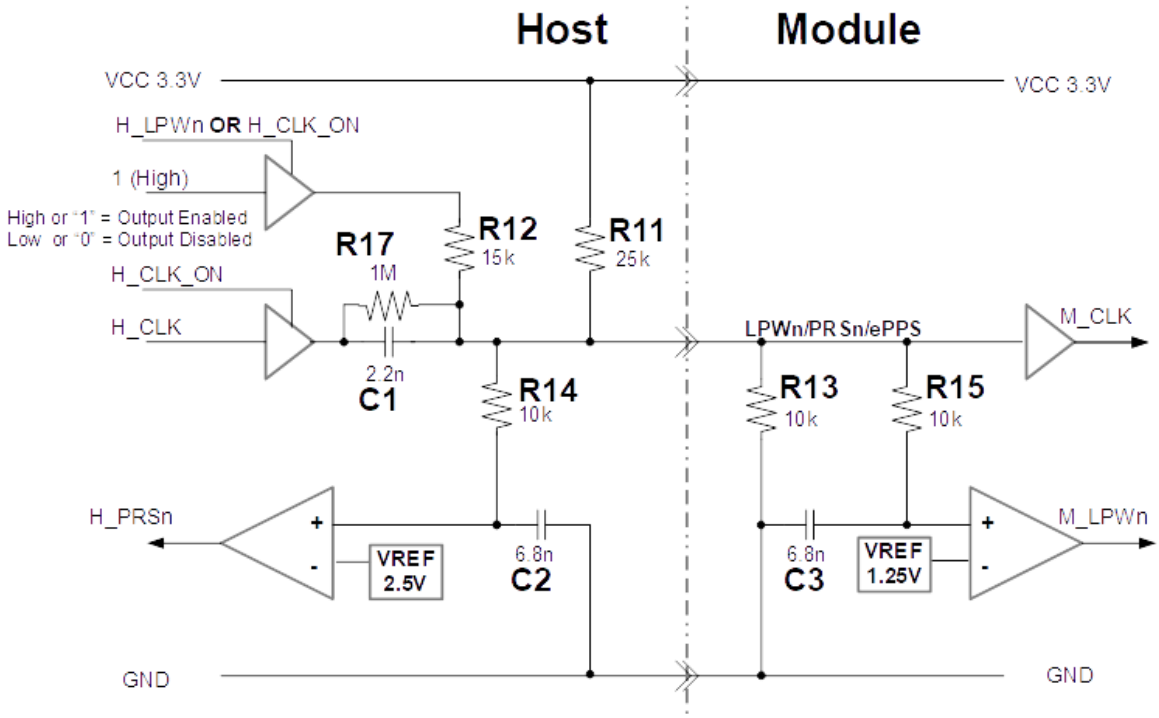


Figure 10-6: LPWn/PRSn/ePPS circuit

In the circuit above, the LPWn/PRSn signal is translated to LPWn/PRSn/ePPS where H_CLK and M_CLK refer to the ePPS/Clock signal.

Table 10-7: LPWn/PRSn/ePPS circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
R14	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
R15	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
R16	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
R17	1M	990k	1.01M	Ohms	Recommend 1M ohms 1% resistor
C1	2.2n	1.98n	2.42n	Farad	Recommend 2.2n farad 10% capacitor
C2	6.8n	6.12n	7.48n	Farad	Recommend 6.8n farad 10% capacitor
C3	6.8n	6.12n	7.48n	Farad	Recommend 6.8n farad 10% capacitor
V_LPWn/PRSn/ePPS _1	0.950	0.000	1.100	Volts	LPWn/PRSn/ePPS voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn/ePPS _2	1.700	1.400	2.250	Volts	LPWn/PRSn/ePPS voltage for Module installed, H_LPWn=High
V_LPWn/PRSn/ePPS_3	3.300	2.750	3.465	Volts	LPWn/PRSn/ePPS voltage for No Module

It is possible for a system to implement PRSn and ePPS Clock without a LPWn signal. Figure 10-7 shows an example of that implementation.

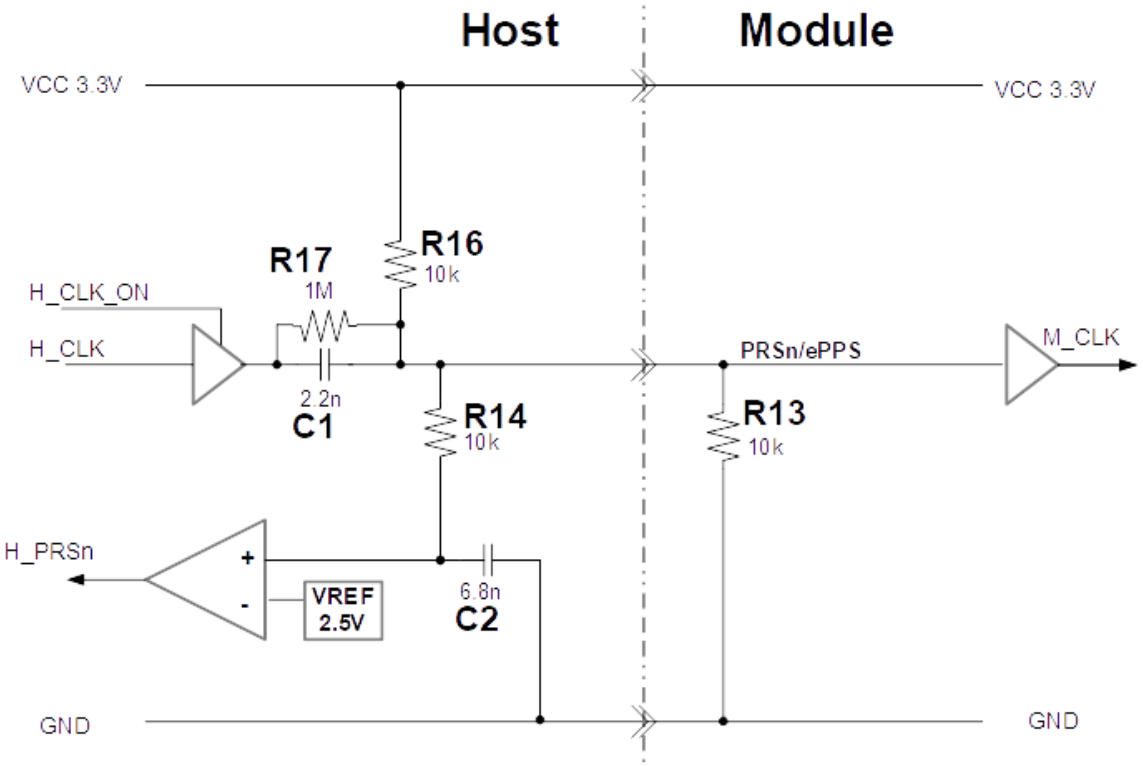


Figure 10-7: PRSn/ePPS circuit

For high-performance Precision Time Protocol (PTP) applications, the ePPS (Enhanced Pulse Per Second) reference with a modulated PPS may be provided from the host to the module for time synchronization. This can be used for either offline delay characterization or real-time delay compensation within the module. The ePPS signal is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter. The ePPS/Clock module input optionally can be configured to provide reference clock to the CDR/DSP. Registers to support optional ePPS/Clock will be added in future revisions of CMIS, but Table 10-8, Table 10-9, Table 10-10, Table 10-11, and Table 10-12 offer a guide for implementors.

Table 10-8: ePPS/Clock Advertising Capabilities

Byte Location (refer to CMIS*)	Bit	Mode Supported
xxxxxx--	00	ePPS/Clock not supported
xxxxxx--	01	ePPS/Clock module supports either 1PPS mode, modulated 1PPS, or clock input for encoding see Table 10-9
xxxxxx--	10	ePPS/Clock supporter TOD (Time of Day)
xxxxxx--	11	ePPS/Clock – Reserved

Table 10-9: ePPS Clock Modes

Byte Location (refer to CMIS*)	Bit	Mode Supported
xxxx--xx	00	RF clock frequency, see Table 10-12
xxxx--xx	01	N/A
xxxx--xx	10	1PPS sent as 75%/25% duty cycle on RF modulated clock, for clock frequency, see Table 10-10
xxxx--xx	11	ePPS/Clock – Reserved

Table 10-10: ePPS Clock Frequency

Byte Location (refer to CMIS*)	Bit	Mode Supported
----xxxx	0000	10 MHz
----xxxx	0001	12.5 MHz
----xxxx	0010	20 MHz
----xxxx	0011	24.576 MHz
----xxxx	0100	25 MHz
----xxxx	0101	156.25 MHz
----xxxx	0110-1101	Reserved
----xxxx	1110-1111	Custom

Table 10-11: Module ePPS/Clock Status Reporting (Req'd if module supports ePPS/Clock)

Byte Location (refer to CMIS*)	Bit	Mode Supported
xxxx--xx	00	ePPS/Clock signals not detected
xxxx--xx	01	N/A
xxxx--xx	10	1PPS modulated signal detected
xxxx--xx	11	Clock signal detected

Table 10-12: ePPS RF or Clock Frequency Reporting (Optional)

Byte Location (refer to CMIS*)	Bit	Mode Supported
----xxxx	0000	10 MHz (ePPS RF)
----xxxx	0001	12.5 MHz (ePPS RF)
----xxxx	0010	20 MHz (ePPS RF)
----xxxx	0011	24.576 MHz (ePPS RF)
----xxxx	0100	25 MHz (ePPS RF)
----xxxx	0101	156.25 MHz (ePPS RF)
----xxxx	0110-1101	Reserved
----xxxx	1110-1111	Custom

* Byte location(s) is not yet listed in CMIS Revision 5.2

10.5.5 Application/Vendor Specific (Optional)

The Application/Vendor Specific signals A/VS1, A/VS2, A/VS3, and A/VS4 provide general purpose IO configurability and extend capabilities for the Host and Module to interact. The definition and application of above signals will be application specific or vendor specific. Application specific IO use cases will be defined by the OSFP MSA or OIF CMIS and vendor specific use cases will be entirely up to the vendors. Compatibility across all applications is not guaranteed and care should be taken to make sure CMIS capabilities of the module are read prior to activating these IOs to prevent damage to the Host or Module.

Some applications, like an Enhanced Serial Gigabit Media Independent Interface (E-SGMII) currently being defined by the OIF PLL Working Group will be documented for consistent support across vendors.

10.5.6 Timing for Control and Status Functions

The CMIS specification should be followed for any timing of control and status functions that have not been defined in this specification.

10.5.7 OSFP-XD Module Power Up Behavior

The OSFP-XD module shall power up when system power is enabled or on module insertion or on VCC power enable to the module. Once powered, the module shall either wait in Low Power mode or enter High Power mode based on the state of the Reset signal, Low Power signal and ForceLowPwr bit of the module. The ForceLowPwr bit default is pre-programmed in the module by the manufacturer and typically would be set to 0. The host can change the ForceLowPwr bit after power up but it shall return to its pre-programmed default when the module is placed in reset or power cycled. The Reset and Low Power signals are described in sections 10.5.2 and 10.5.3. The ForceLowPwr bit is defined in the OSFP-XD Management Interface Specification.

The table below shows the module power up state based on Low Power and ForceLowPwr. If LPWn=0 then the module shall go to low power mode and transmitters disabled. If ForceLowPwr=0 and LPWn=1 then the module shall immediately enable transmitters. If ForceLowPwr=1 and LPWn=1 then the module shall wait in Low Power mode until the host clears the ForceLowPwr bit for the module to enable transmitters.

Table 10-13: Power up behavior

Module State	**ForceLowPwr = 0**	**ForceLowPwr = 1**
Low Power asserted (LPWn = 0)	Low Power Mode (transmitters Disabled)	Low Power Mode (transmitters Disabled)
Low Power de-asserted (LPWn = 1)	Operational (transmitters Enabled*)	Low Power Mode (transmitters Disabled)

*The host may use the management interface to alter this default behavior

10.5.8 OSFP-XD Module Reset Behavior

Reset is a hardware signal from the INT/RSTn pin as defined in section 10.5.2. Asserting Reset overrides all other hardware and software controls and forces the module into the Reset state. This includes forcing Low Power mode and disabling transmitters.

10.6 Power

+3.3V power is delivered to the module via 8 power pins (VCC). These 8 power pins shall be connected on both the module and the host. Each power pin allows up to 2.5 Amps for a total of 20 Amps. This enables a maximum power in excess of 60 Watts.

The specification of the module power is in accordance with methods defined by SFF-8679 Rev 1.7 section 5.5. There are 8 power classes defined as shown in Table 10-15. All modules in reset or the default low power mode must comply with Power Class 1. High power mode enables the module to draw power up to its advertised power class, and may be conditionally enabled by the host. The host may read the module power class register to know the power class of the module before or after enabling high power mode. The module shall not exceed the power class it identifies for itself.

Transition between low and high power mode is controlled by the M_RSTn (reset) signal, M_LPWn (low power mode) signal and ForceLowPwr bit. The module shall remain in or transition to low power mode when M_LPWn or M_RSTn are asserted or the ForceLowPwr bit is set. While in low power mode, active modules shall also disable transmitters. The module may transition to high power mode once M_RSTn and M_LPWn are deasserted and the ForceLowPwr bit is cleared.

The specifications of Table 10-14 and Table 10-15 are for the combined power of all 8 power pins. The measurement location for these specifications is at the OSFP-XD connector VCC pins on the host board.

Table 10-14: OSFP-XD power specification

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.201	3.300	3.465	V
Voltage drop across mated connector (Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV
Total current for Vcc pins (1)	Icc_module			20	A
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (2)	I_didt			100	mA/µs
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs

(1) Utilization of the maximum OSFP-XD power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

(2) The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power and high-power to low-power.

Table 10-15: OSFP-XD power classes

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Low Power Mode – M_LPWn or M_RSTn asserted or ForceLowPwr					
Power consumption	P_lp			2	W
Instantaneous peak current at hot plug	Icc_ip_lp			800	mA
Sustained peak current at hot plug	Icc_sp_lp			666	mA
Steady state current (1)	Icc_lp			637	mA
Power Class 1 module (high power mode)					
Power consumption	P_1			1.5	W
Instantaneous peak current at hot plug	Icc_ip_1			600	mA
Sustained peak current at hot plug	Icc_sp_1			500	mA
Steady state current (1)	Icc_1			478	mA
Power Class 2 module (high power mode)					
Power consumption	P_2			3.5	W
Instantaneous peak current at high power enable	Icc_ip_2			1400	mA
Sustained peak current at high power enable	Icc_sp_2			1167	mA
Steady state current (1)	Icc_2			1116	mA
Power Class 3 module (high power mode)					
Power consumption	P_3			7	W
Instantaneous peak current at high power enable	Icc_ip_3			2800	mA
Sustained peak current at high power enable	Icc_sp_3			2333	mA
Steady state current (1)	Icc_3			2233	mA
Power Class 4 module (high power mode)					
Power consumption	P_4			8	W
Instantaneous peak current at high power enable	Icc_ip_4			3200	mA
Sustained peak current at high power enable	Icc_sp_4			2666	mA
Steady state current (1)	Icc_4			2552	mA
Power Class 5 module (high power mode)					
Power consumption	P_5			10	W
Instantaneous peak current at high power enable	Icc_ip_5			4000	mA
Sustained peak current at high power enable	Icc_sp_5			3333	mA
Steady state current (1)	Icc_5			3190	mA
Power Class 6 module (high power mode)					
Power consumption	P_6			12	W
Instantaneous peak current at high power enable	Icc_ip_6			4800	mA
Sustained peak current at high power enable	Icc_sp_6			4000	mA
Steady state current (1)	Icc_6			3828	mA
Power Class 7 module (high power mode)					
Power consumption	P_7			14	W
Instantaneous peak current at high power enable	Icc_ip_7			5600	mA
Sustained peak current at high power enable	Icc_sp_7			4666	mA
Steady state current (1)	Icc_7			4466	mA
Power Class 8 module (high power mode)					
Power consumption	P_8 (2)			>14	W
Instantaneous peak current at high power enable	Icc_ip_8			P_8 * 400	mA
Sustained peak current at high power enable	Icc_sp_8			P_8 * 333	mA
Steady state current (1)	Icc_8			7600	mA

(1) Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

(2) Power consumption P_8 is readable from the module Max Power register as defined in the Management Specification.

As a reference, Table 10-16 will track the maximum power allowed in the previous revisions in the OSFP-XD MSA.

Table 10-16: OSFP-XD power summary per MSA revision

OSFP-XD MSA Rev	Max Current	Max Power (at 3.3V nominal)
1.0	20 A	66 W

10.6.1 Power Filter

Figure 10-8 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

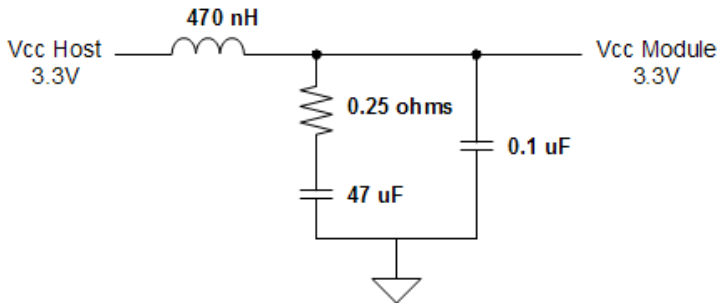


Figure 10-8: Host board power filter circuit

10.6.2 Power Electronic Circuit Breaker (optional)

For safety and protection of the host system, the power to each OSFP-XD module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP-XD connector.

10.7 Examples of OSFP-XD Host Board and Module Block Diagram

Figure 10-9, Figure 10-10, Figure 10-11, and Figure *10-12* show examples of OSFP-XD/XD-8 host board connections to the module. The examples included in this section are not exhaustive, and alternative interfaces are possible at the discretion of the implementor.

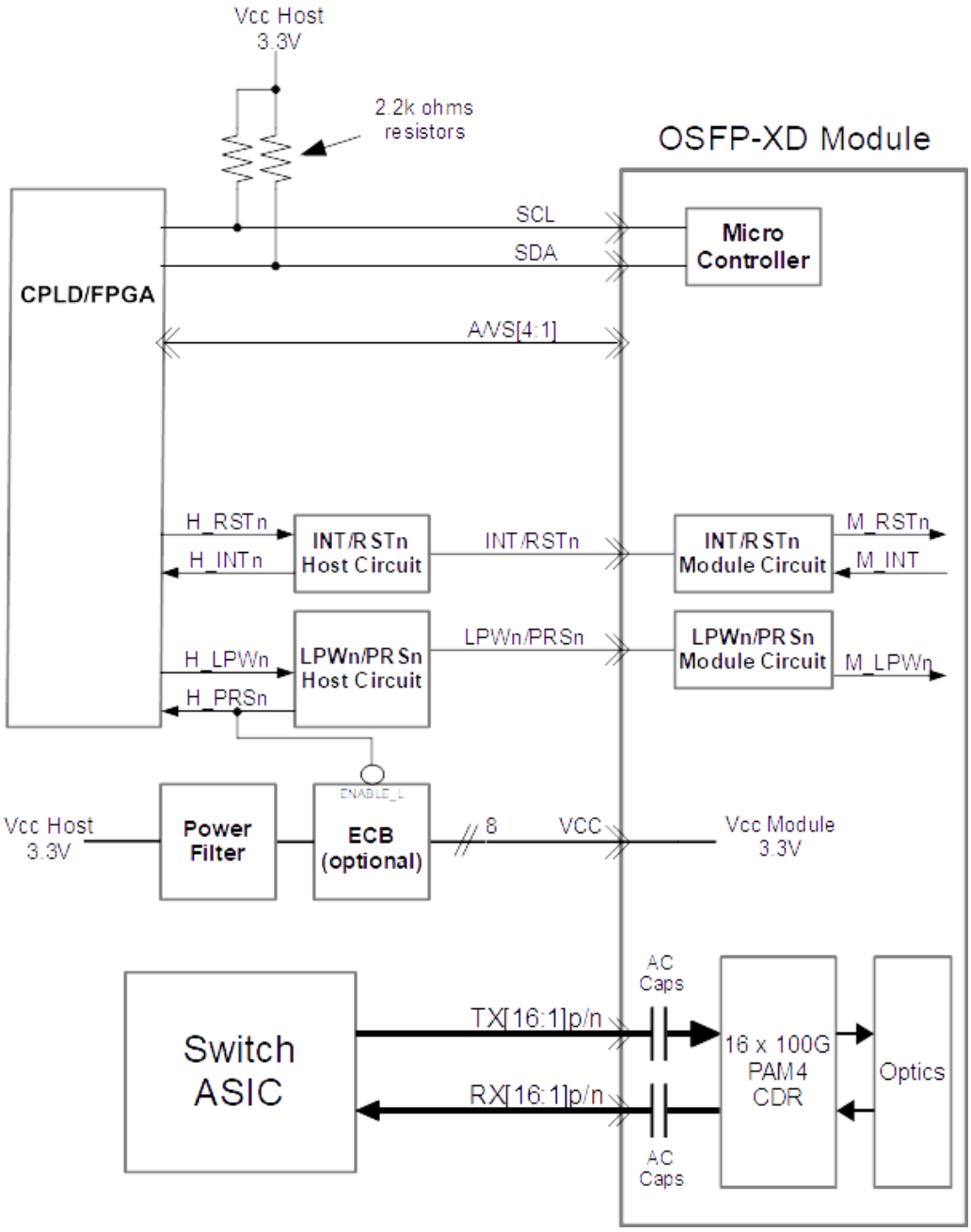


Figure 10-9: Typical OSFP-XD Host board and Module block diagram

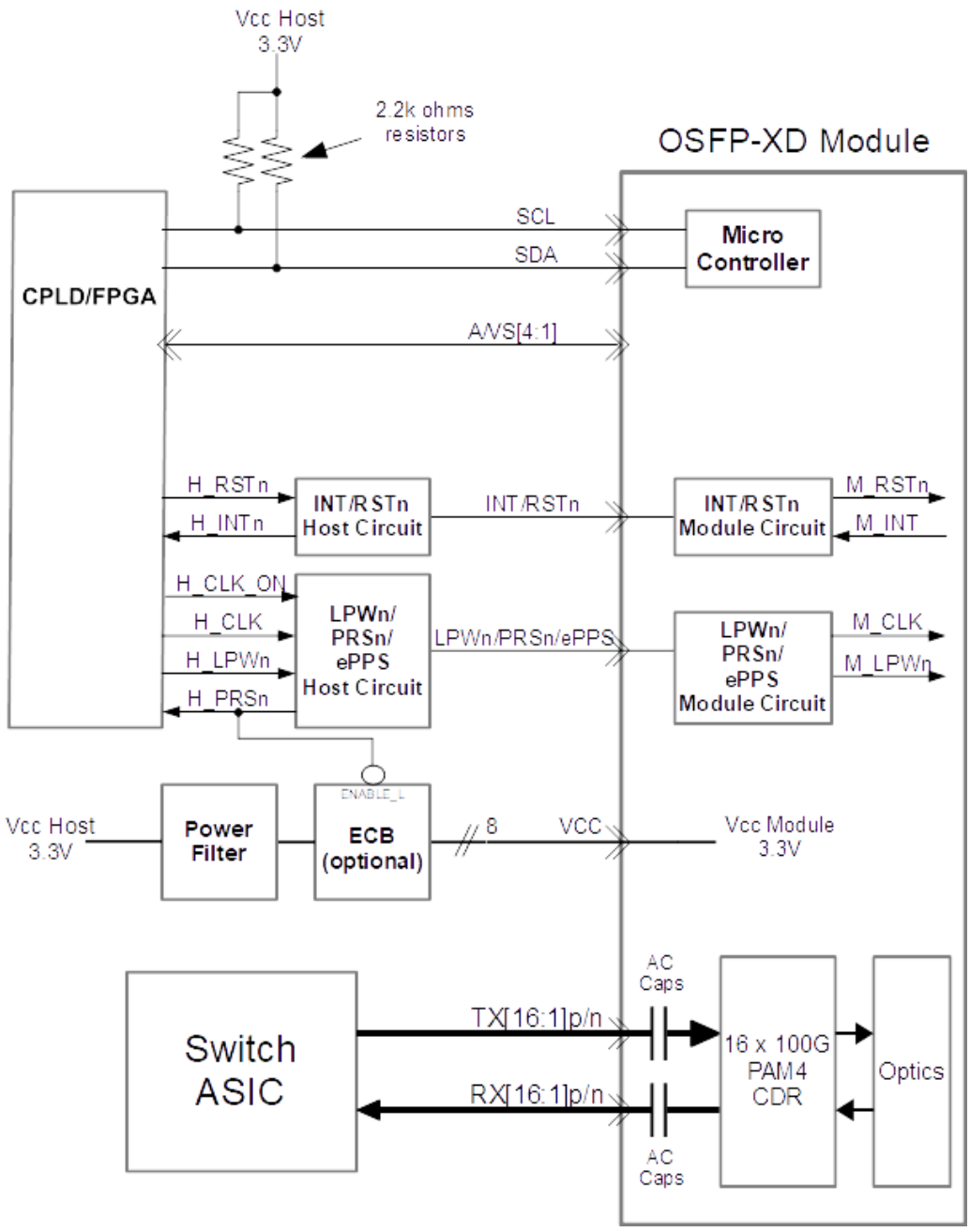


Figure 10-10: OSFP-XD Host board and Module block diagram with support for ePPS/Clock

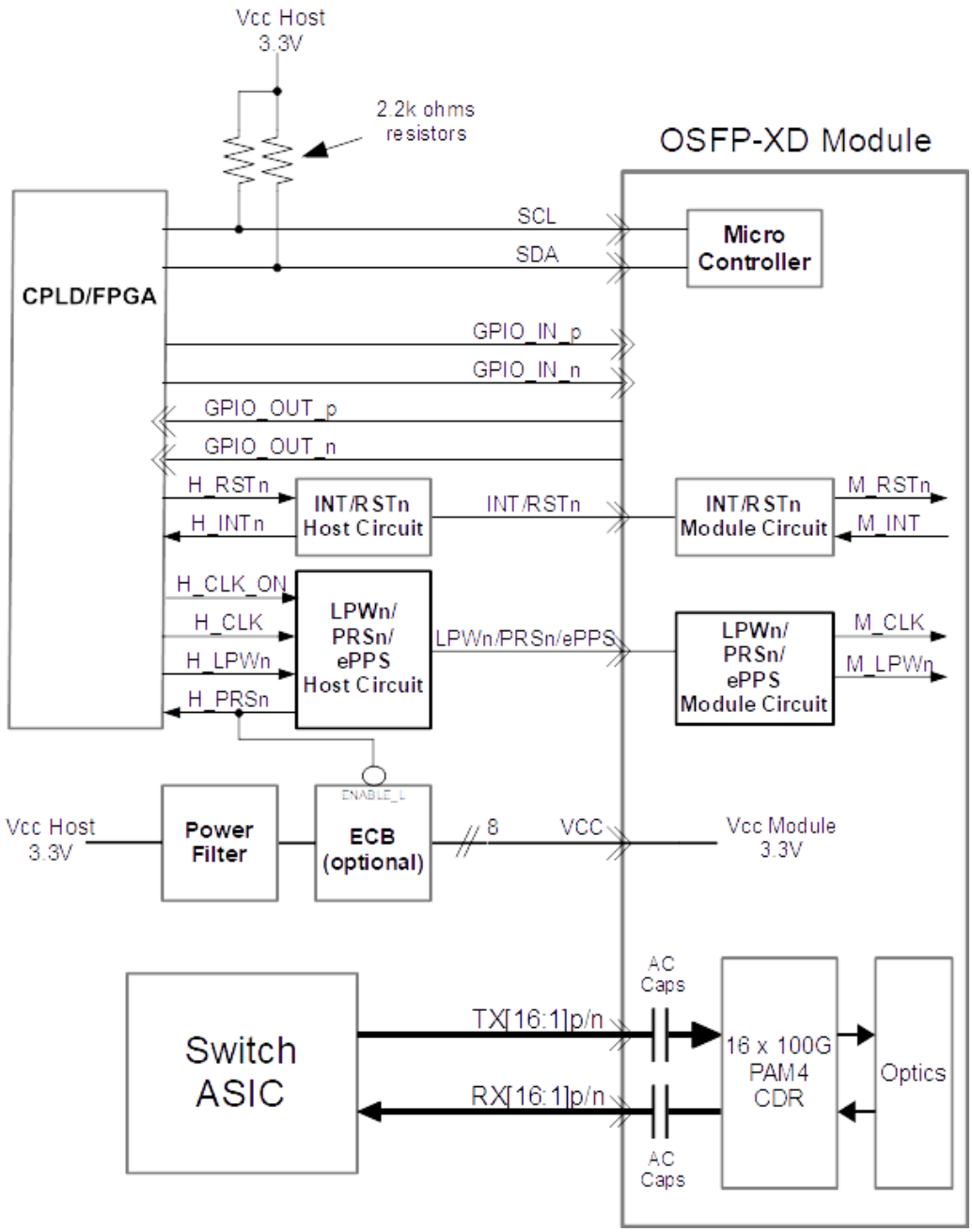


Figure 10-11: OSFP-XD Host board and Module block diagram with support for ePPS/Clock and future E-SGMII.*

* E-SGMII and ePPS/Clock support are currently under active development at the OIF

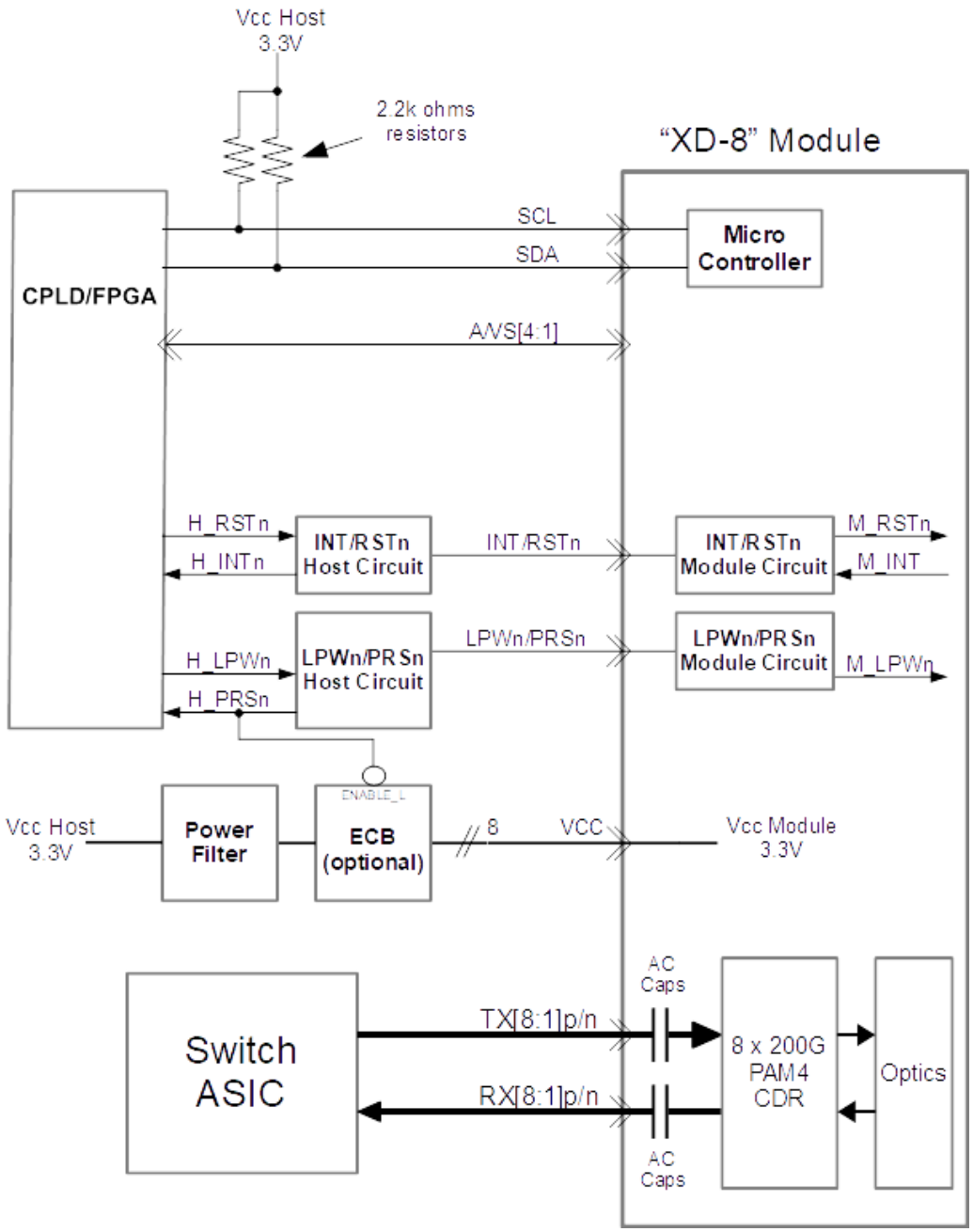


Figure 10-12*: Typical XD-8 Host board and Module block diagram.*

10.8 Electrostatic Discharge (ESD)

Where ESD performance is not otherwise specified, the OSFP-XD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

The OSFP-XD module and host high-speed signal, low-speed signal and power contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

Appendix A. Cage Flap Location Inspection Gauge

A.1 Example of the Cage Flap Location Inspection Gauge

In Figure 4-25 and Figure 8-22, the location of the cage flap with respect to the cage positive stop is specified. The location dimension can be measured with a physical gauge or measured under unmated condition and then converted for the flap under mated height (flap deflected to 0.95 mm symmetrically). There is no restriction on how to inspect and measure the flap location if it meets the specification.

A reference design of a gauge tool is shown as in the Figure A-1. Gauge for the OSFP-XD-RHS differ only on its thickness. While the dimension “A” reproduces the mated condition, Dimension B will center align the gauge inside the cage.

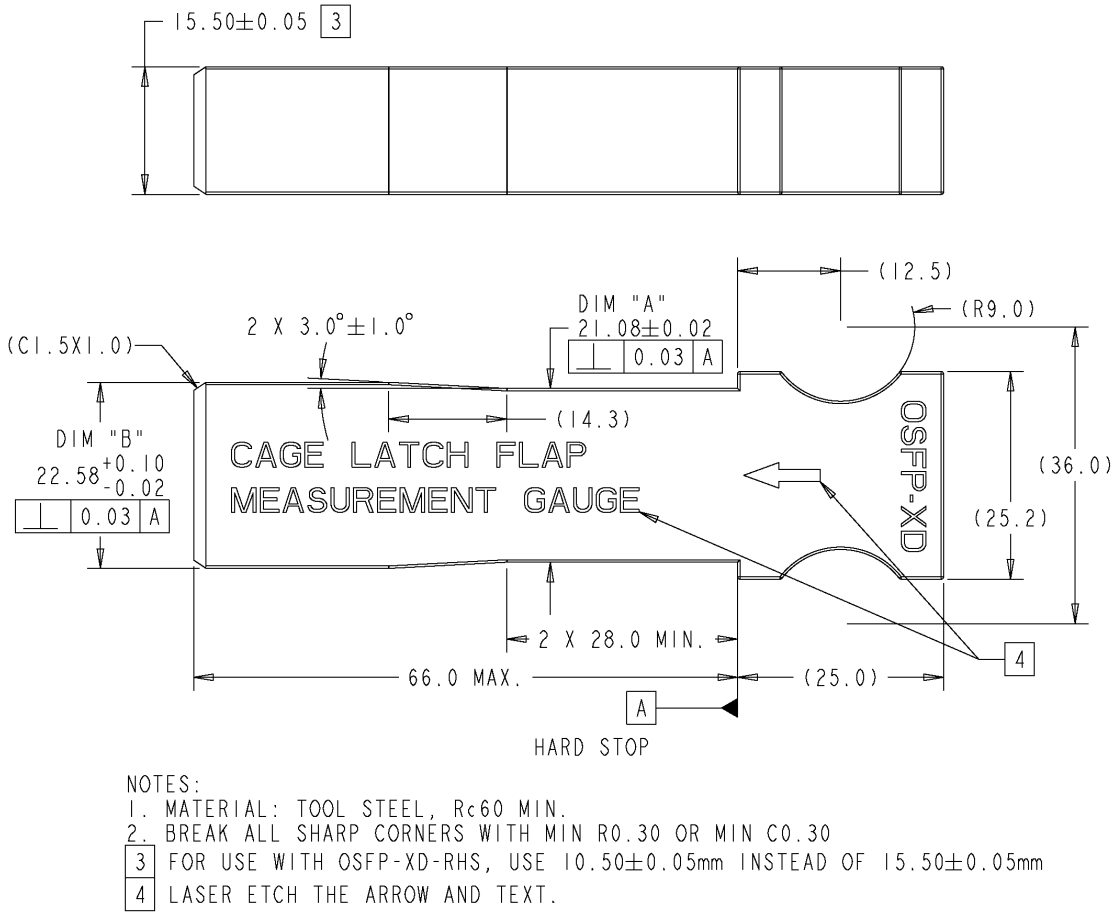


Figure A-1: OSFP-XD and OSFP-XD-RHS Cage flap location inspection gauge (Reference)

Appendix B. Cross-Incompatibility of OSFP and OSFP-XD

OSFP-XD module is a pluggable module with 16 channels, which is twice of the OSFP. OSFP and OSFP-XD modules are not compatible.

Figure B-1 shows comparison of the OSFP and OSFP-XD. Figure B-2 shows that the OSFP-XD is taller than the OSFP. Figure B-3 shows that the OSFP-XD is taller, and also the connector mating paddle card design is different.

Mechanical keying prevents insertion of OSFP-XD modules into OSFP ports, and OSFP modules into OSFP-XD ports. These modules and ports combinations are incompatible. Despite the keying features, abuse and forced insertion of a module to wrong port can cause a mechanical damage to the port.

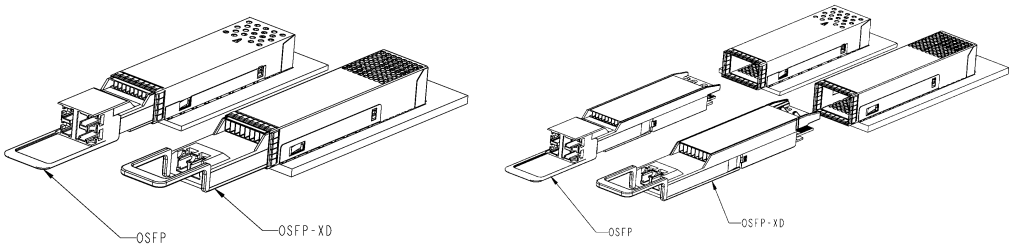


Figure B-1: OSFP and OSFP-XD, module and port

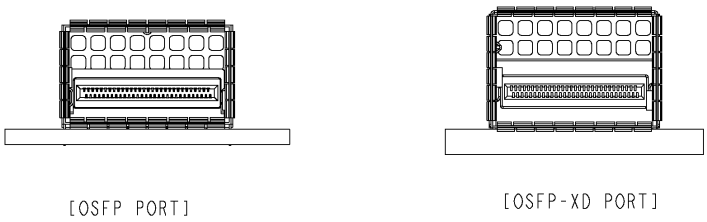


Figure B-2: OSFP and OSFP-XD, port front view

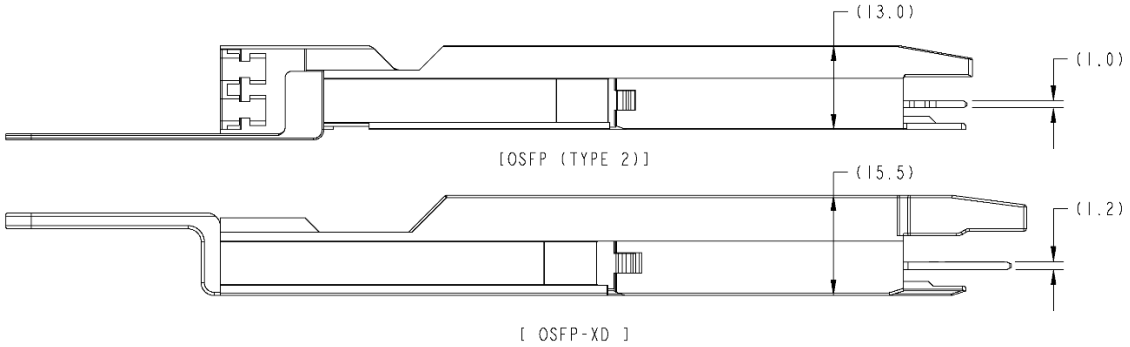


Figure B-3: OSFP and OSFP-XD, module side view

Appendix C. Thermal Monitoring for High Power Modules

** This section is adopted from the QSFP-DD Hardware specification Rev 7.1, Section 9.4.*

C.1 Thermal Characteristics for High Power Modules

In high power modules, the module implementer needs to ensure that the module meets all performance and reliability specifications and monitoring only the case temperature can result in overly conservative readings for the host equipment to use. Instead by monitoring all necessary internal component temperature sensors against their high temperature warning/alarm/shutdown limits, the module and host equipment can more accurately assess the component's margin to the various temperature limits that affect performance and reliability. To be compatible with the existing CMIS approach to report the case temperature Tcase, it is possible to convert these multiple sensor readings in such a way to provide the host equipment the ability to manage the system and module cooling without a change to CMIS software. The specific temperature sensors, including their values, thresholds and physical location are defined and known by the module implementor, and are not required to be advertised to the equipment supplier. Instead, the module's firmware shall process the monitored temperature data points against their limits, and provide the following to the equipment supplier via the management interface:

A high temperature monitor, which shall be a single monotonic increasing/decreasing value and be a consolidated leading indicator for all the module's defined sensor points against their high temperature thresholds (including warning, alarm, shutdown).

Module implementor's defined limits for the high temperature monitor values, including warning, alarm and shutdown thresholds are known. The least margin to these limits shall be advertised to the equipment supplier as the equivalent margin to the advertised case temperature limit via the management interface. The module's specified case temperature limits are recommended (but not required) to be consistent with temperature ranges classes defined in section 7.1.

The temperature monitors are expected to represent an accurate measurement of where the module operates relative to the temperature limits defined by the module supplier. The temperature monitors are not expected to represent a physical temperature at any specified location on or inside the module.

C.2 Example Procedure to Implement High Power Module Monitoring (Optional)

As an example, a procedure to calculate the high temperature case monitor temperature alarm threshold that is reported by the module in CMIS to the host is outlined below in a case where 3 temperature sensors are being monitored by the module firmware (laser, DSP, TIA):

Step I:

The module's case temperature monitored sensor reading (Tcase) should have internal module specified thresholds that are advertised via the management interface:

$Tcase_{warning\ threshold}$:Module case temperature warning threshold (for example 70 ºC)

$Tcase_{alarm\ threshold}$: Module case temperature alarm threshold (for example 75 ºC)

$Tcase_{shutdown\ threshold}$: Module case temperature shutdown threshold (for example 80 ºC)

Step II:

Including all monitored sensors, calculate the temperature margin for the leading indicator against the module's known internal warning, alarm and shutdown thresholds.

$margin_{warning}$ = min($Dt_{laser,\ warning}$, $Dt_{DSP,warning}$, $Dt_{tia,warning}$, … etc.)
$margin_{alarm}$ = min($Dt_{laser,\ alarm}$, $Dt_{DSP,alarm}$, $Dt_{tia,alarm}$, … etc.)
$margin_{shutdown}$ = min($Dt_{laser,\ shutdown}$, $Dt_{DSP,shutdown}$, $Dt_{tia,shutdown}$, … etc.)
Where $Dt_{A,B}$ is the temperature margin for sensor A against its high temperature B threshold (where B can be the warning, alarm or shutdown temperature threshold).

The calculation of the reported case temperature reading (Tcase) should be agnostic to how the module design defines the temperature thresholds of the monitored sensors, including temperature steps between warning, alarm and shutdown thresholds. One implementation that can accomplish this is outlined in step III below.

Step III:
Based on the margin with the smallest value greater or equal to zero, calculate the reported Tcase as below.
If $margin_{warning}$ is the smallest margin, greater or equal to 0:
$Tcase_{warning} = Tcase_{warning\ threshold} - margin_{warning}$
If $margin_{alarm}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{alarm threshold}} - margin_{\text{alarm}} * \frac{Tcase_{\text{alarm}} - Tcase_{\text{warning}}}{t_{\text{A,alarm}} - t_{\text{A,warning}}}$$

where $t_{\text{A,alarm}}$ and $t_{\text{A,warning}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.
If $margin_{shutdown}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{shutdown threshold}} - margin_{\text{shutdown}} * \frac{Tcase_{\text{shutdown}} - Tcase_{\text{alarm}}}{t_{\text{A,shutdown}} - t_{\text{A,alarm}}}$$

where $t_{\text{A,shutdown}}$ and $t_{\text{A,alarm}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.